S/N 10/751,091   <u>PATENT</u>

<u>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</u>

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

Electronically filed on March 23, 2009.

<u>APPELLANT'S BRIEF ON APPEAL</u>

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

    This Brief is presented in support of the Appeal filed January 23, 2009, from the final rejection of Claims 65-68 and 71-75 of the above-identified application, as set forth in the Office Action mailed September 24, 2008.

    Payment is being made via credit card in the amount of $270 to cover the required fee for filing this Brief.

    An oral hearing is requested. A separate request for oral hearing with the appropriate fee will be filed within two months of the Examiner's Answer.

I. REAL PARTY OF INTEREST

The real party in interest is the Superconductor Technologies Inc. of Santa Barbara, California.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 65-68 and 71-75 are pending and stand rejected. Claims 1-64 and 69-70 have been cancelled. Claims 65-68 and 71-75 are on appeal and are listed in the CLAIMS APPENDIX.

IV. STATUS OF AMENDMENTS

As of the Final Rejection, mailed on 24 September 2008[1], claims 1-74 were pending, of which claims 22-58 had been withdrawn. Applicants have filed three (3) amendments, each time from the claims as of the Final Rejection, subsequent to the Final Rejection:

      1. Applicants amended claims 63-74 and added claims 75 and 76 by an Amendment filed on 9 October 2008. The Amendment was acted upon by the Advisory Action of 24 October 2008 but **not entered**.

      2. Applicants amended claims 63-68 and 71-74, cancelled claims 69-70, and added claims 75 by an Amendment filed on 18 November 2008. The Amendment was acted upon by the Advisory Action of 2 December 2008 but **not entered**.

      3. Applicants amended claims 65-68 and 71-74, cancelled claims 1-64 and 69-70, and added claims 75 by an Amendment filed on 5 December 2008. The Amendment was acted upon by the Advisory Action of 19 December 2008 and **entered**.

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[1] An Office Action was mailed on 18 August 2008. However, in that Office Action, only claims 1-64 was addressed and finally rejected. A second Office Action, addressing all claims in the Applicants' Amendment of 14 August 2008, was mailed on 24 September 2008 and is the basis for the present appeal. Unless otherwise noted, "Final Rejection" shall hereinafter refer to the 24 September 2008 Office Action.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

In the following summary, Appellants provide exemplary references to sections of the specification and/or drawings supporting the subject matter as defined in the claims as required by 37 C.F.R. § 41.37(c)(1)(v). The specification and drawings also include additional support for other exemplary embodiments encompassed by the claimed subject matter. Thus, it should be appreciated that the references are not exhaustive and are intended only to be illustrative in nature.

A. Independent Claim 65

Appellants note that the language of claim 65 defines the scope of the subject matter of the claim. The summary below is intended for the convenience of the Board and is not intended to limit the scope of the claim.

Claim 65 recites a Josephson junction device. *See, e.g.,* Figure 1; p. 7, lines 11-14; . The Josephson junction is one of the basic elements of superconductor electronic devices, and is well-developed in low temperature superconductors. *See, e.g.,* p. 3, line 14-15. The invention claimed in the claim 65 relates to a Josephson junction device using high-temperature superconductors. The device comprises:

a first layer comprising an oxide high-temperature superconductor (*e.g.,* the layer reference labeled "12" in Figure 1; p. 10, lines 23-27);

a second layer comprising an oxide high-temperature superconductor (*e.g.,* the layer reference labeled "18" in Figure 1; p. 11, lines 5-7; p. 12, lines 13-14); and

a third layer (*e.g.,* the layer reference labeled "20" in Figure 1) connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer (p. 11, line 21-23 (the exposed surface layer 20 of the high-temperature superconductor layer is converted to a layer of a difference phase, structure or chemical composition.)),

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the device having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K (*see, e.g.,* Figure 6 and p. 13, lines 5-9).

It should be noted that support for claim 65 also lies in other portions of the written description as well as in other figures. For clarity, Appellant only cites to the above portions of the specification and figures.

B. Independent Claim 67

Appellants note that the language of claim 67 defines the scope of the subject matter of the claim. The summary below is intended for the convenience of the Board and is not intended to limit the scope of the claim.

Claim 67 recites an electronic device comprising:

a crystalline substrate (Ref. 10 in Figure 1; p. 10, line 9-16);

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide (e.g., the layer reference labeled "12" in Figure 1; p. 10, line 23-p. 11, line 27);

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide (e.g., the layer reference labeled "20" in Figure 1; p. 11, line 21-23 (the exposed surface layer 20 of the high-temperature superconductor layer is converted to a layer of a difference phase, structure or chemical composition.)); and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide (*e.g.,* the layer reference labeled "18" in Figure 1; p. 11, lines 5-7; p. 12, lines 13-14; p. 7, lines 15-20; original claim 1), whereby a Josephson junction is formed between the electrode and the counter-electrode, having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K (*see, e.g.,* Figure 6 and p. 13, lines 5-9).

It should be noted that support for claim 67 also lies in other portions of the written description as well as in other figures. For clarity, Appellant cites only to the above portions of the specification and figures.

C. Independent Claim 71

Appellants note that the language of claim 71 defines the scope of the subject matter of the claim. The summary below is intended for the convenience of the Board and is not intended to limit the scope of the claim.

Claim 71 recites a Josephson junction device. *See, e.g.,* Figure 1; p. 7, lines 11-14; . The Josephson junction is one of the basic elements of superconductor electronic devices, and is well-developed in low temperature superconductors. *See, e.g.,* p. 3, line 14-15. The invention claimed in the claim 65 relates to a Josephson junction device using high-temperature superconductors. The device comprises:

a first layer comprising an oxide high-temperature superconductor (*e.g.,* the layer reference labeled "12" in Figure 1; p. 10, lines 23-27);

a second layer comprising an oxide high-temperature superconductor (*e.g.,* the layer reference labeled "18" in Figure 1; p. 11, lines 5-7; p. 12, lines 13-14); and

a third layer (*e.g.,* the layer reference labeled "20" in Figure 1) connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer (p. 11, line 21-23 (the exposed surface layer 20 of the high-temperature superconductor layer is converted to a layer of a difference phase, structure or chemical composition.)),

the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K. (*See, e.g.,* Figure 6 and p. 13, line 5-19.)

It should be noted that support for claim 71 also lies in other portions of the written description as well as in other figures. For clarity, Appellant only cites to the above portions of the specification and figures.

D. Independent Claim 73

Appellants note that the language of claim 73 defines the scope of the subject matter of the claim. The summary below is intended for the convenience of the Board and is not intended to limit the scope of the claim.

Claim 73 recites an electronic device comprising:

a crystalline substrate (Ref. 10 in Figure 1; p. 10, line 9-16);

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide (e.g., the layer reference labeled "12" in Figure 1; p. 10, line 23-p. 11, line 27);

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide (e.g., the layer reference labeled "20" in Figure 1; p. 11, line 21-23 (the exposed surface layer 20 of the high-temperature superconductor layer is converted to a layer of a difference phase, structure or chemical composition.)); and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide (e.g., the layer reference labeled "18" in Figure 1; p. 11, lines 5-7; p. 12, lines 13-14; p. 7, lines 15-20; original claim 1), whereby a Josephson junction is formed between the electrode and the counter-electrode,

the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K (*See, e.g.,* Figure 6 and p. 13, line 5-19.).

It should be noted that support for claim 73 also lies in other portions of the written description as well as in other figures. For clarity, Appellant cites only to the above portions of the specification and figures.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 65-68 and 71-75 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Harada* (K. Harada, H. Myoren, and Y. Osaka, "Fabrication of all-high-Tc Josephson junction using as-grown $YBa_2Cu_3O_x$ thin films," Jap. J. Appl. Phys., vol. 30, pp. L1387, 1991) in view of *Chan* (U.S. Pat. No. 5,892,243) and either one of *Hunt* (Hunt, B. *et al.,* "High Temperature Superconductor Weak Links", *Second Symposium on Low Temperature Electronics and High Temperature Superconductivity,* Electrochemical Society Meeting, Honolulu, Hawaii, Vol. 93-22, p. 467-472 (May 1993)) and *Jia* (C.L. Jia *et al.,* "Effect of chemical and ion-beam etching on the atomic structure of interfaces in $YBa_2Cu_3O_7/PrBa_2Cu_3O_7$ Josephson junctions", *Appl. Phys. Lett.,* Vol 67, No. 24, 3635-3637 (1995)).

The Examiner appeared to take the position in the Advisory Action of 19 December 2009 that the references above were used in the same way that they were used to reject claims 1-5, 7-21 and 59-74. However, only *Jia* was used in combination with *Harada* and *Chan* in rejecting claims 65-74 in the Final Rejection, while *Hunt* was only included in rejecting other claims. Nonetheless, Applicants will explain below why the appealed claims are patentable even if *Hunt* were also applied.

VII. ARGUMENT

All of the pending independent claims have been finally rejected under 35 U.S.C. § 103(a). 35 U.S.C. § 103 states: "A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." According to the U.S. Supreme Court in *KSR International Co. v. Teleflex*, "[r]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the **predictable** use of prior art elements according to their established functions." *Id.* at 1740 (emphasis added). (*See, also, MPEP* § 2141.)

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), the references must teach or suggest all of the claimed limitations to one of ordinary skill in the art at the time the invention was made. *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974); *In re Wilson*, 424 F.2d 1382, 1385 (C.C.P.A. 1970); *Ex Parte Wada and Murphy*, BPAI Appeal No. 2007-3733 (January 14, 2008) (quoting *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) and *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003)). *See also*, M.P.E.P § 2143.03 ("All claim limitations must be considered.") Appellants submit that the Examiner has failed to state a *prima facie* case for rejecting the independent claims, and all rejections should be withdrawn and the application allowed in its current form.

    A. <u>The *Harada, Chan, Hunt and Jia* References, Individually or in Combination, Fail to Teach or Suggest All Claim Limitations of Any Independent Claim, Nor are the Missing Limitations Predictable Results of Modification of Prior Art by Any Known Method.</u>

Each of the appealed independent claims includes, among other things, two features: (a) that the layer ("third layer" in claims 65 and 71, and "barrier" in claims 67 and 73) intervening the two high-temperature superconductor layers is an ion-modified layer or portion of one of the

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superconductor layers; that each independent claim includes an electrical property of the device at a temperature of 4.2K: a range of R_nA (normalized junction resistance (*see,* p. 3, lines 18-20 of the Specification)) for claims 65 and 67, and a range of J_c (critical current density (*see, id.*))

None of the cited references discloses or suggests the R_nA range or J_c range recited in these claims at 4.2K. The Examiner point to *Hunt* as disclosing an R_nA of 2.9×10^{-9} Ω-cm^2 and J_c of 5×10^4 A/cm^2, citing *Hunt* at p. 9. Final Rejection at Continuation Sheet. However, *Hunt* clearly indicates at the cited portion that the temperature at which the R_nA and J_c values were obtained was 77 K, far higher than the 4.2 K specified by the appealed claims. For temperature of 4.2 K, *Hunt* discloses an R_nA value of only 5×10^{-10} Ω-cm^2 for junctions made of ion-damaged layer. *See, Hunt* at page 007. As discussed at least at page 4, lines 25-29 of the Specification, junctions with low R_nA values imply high J_c values for usefully high I_cR_n products, and the J_c in relevant prior art devices is typically too high for applications such as single flux quantum (SFQ) logic devices. For example, *Hunt* discloses a J_c of 5.5×10^6 A/cm^2 and states that a "potential problem is that the device current densities are approaching the electrode J_c values." *See, Hunt* at page 006. That is, J_c values are too high, and the junction is not a weak link at all. In contrast, the claimed devices possess high R_nA values and correspondingly low J_c values, such as 5×10^6 A/cm^2 or lower. Therefore, contrary to the Examiner's assertions, *Hunt* does not disclose or suggest the claim limitations regarding R_nA range or J_c range.

Furthermore, the invention, including its aspect of the combination of ion-modified superconductor layer as barrier and the specific R_nA range or J_c range, claimed in the appealed claims is not a predictable result of modifying the teachings of any of the cited references, alone or in combination.

Regarding *Harada,* it fails to disclose or suggest a barrier that is an ion-modified layer of superconductive oxide electrode. In fact, instead of forming a non-superconducting barrier by ion modification of the superconductive electrode, the purpose of the plasma processing in Harada is to remove contaminants and other nonsuperconducting phase. See, page L1388. Any epitaxial relationship between the electrode and counterelectrode in the structure disclosed in Harada is due to the fact that they were both grown on the same single crystalline MgO substrate. See, page L1388. To further illustrate this point, Applicants further submitted with the Amendment of 28 April 2008 the Declaration of John M. Rowell under 37 C.F.R. § 1.132.

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Professor Rowell is an expert in the relevant technology. As the National Academy of Science notes in its citation, Prof. Rowell "is known for his contributions to the basic understanding and applications of superconductivity: the first observation of the Josephson effect; the quantitative verification of the electron-phonon interaction as the mechanism responsible for conventional superconductivity; and the translation of these accomplishments to applications of both low and high Tc superconductors." (*See,* National Academy of Science Member Directory, accessible at http://www.nasonline.org/site/Dir/38394961?pg=vprof&mbr=1004919&returl=http%3A%2F%2 Fwww.nasonline.org%2Fsite%2FDir%2F38394961%3Fpg%3Dsrch%26view%3Dbasic&retmk= search_again_link.) As Prof. Rowell notes in his Declaration, it is not clear from *Harada* that a barrier made of an ion-modified surface layer of a high-T, superconductor was produced. The conclusion is due at least to (a) poor Josephson junction reported by Harada, (b) the ambiguous statements made in Harada regarding the plasma treatment, and (c) Harada's report of using the lift-off technique to expose the surface to be treated by plasma. Furthermore, Prof. Rowell stated that simply experimenting with the process reported by Harada paper would not have lead to the Josephson junction disclosed and claimed in the present application.

Regarding *Chan,* it only discloses a *deposited* barrier. See, e.g., col. 8, lines 3-1 1 of *Chan.* Chan therefore teaches away from the claimed invention.

As to *Jia,* the Examiner contends that it discloses a substantially similar process of making the barrier layer as that of the claimed invention such that the properties of the barrier layer of *Jia* are substantially similar to the properties of the barrier layer of the claimed invention. Final Rejection at 4. Applicants respectfully disagree with the Examiner. *Jia* discloses a Josephson junction with a layered structure of $YBa_2Cu_3O_7/PrBa_2Cu_3O_7/YBa_2Cu_3O_7$, in which the $PrBa_2Cu_3O_7$ layer is a *deposited* non-superconducting barrier. *See, e.g., id* at Abstract (..."Josephson junctions formed by epitaxial $YBa_2Cu_3O_7/PrBa_2Cu_3O_7/YBa_2Cu_3O_7$ triple-layer films ...") and p. 3635, left column, first paragraph ("In most cases $PrBa_2Cu_3O_7$ is employed as nonsuperconducting barrier material.") The method disclosed in the present application and resulting in the device claimed in appealed claims, in contrast, produces a barrier layer that is ion-modified from one of the superconductor electrodes. Therefore, the process in *Jia* is very different from that of the claimed invention such that the properties of the barrier layer of *Jia* cannot be predicted to be substantially similar to the properties of the barrier layer of

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the claimed invention. Moreover, in order for a device to be classified as a Josephson junction, it must display Josephson properties when measured electrically. *Jia* presents no electrical measurements, no measured values of I_c or R_n, and no evidence that the structures discussed operate as Josephson junctions. Thus, like *Chan, Jia* teaches away from the claimed invention.

Regarding *Hunt*, it fails to disclose or suggest how to modify the junction properties. In fact, at the bottom of page 4 of *Hunt, Hunt* states that "the critical current densities of the ion-damage weak links appear to be relatively insensitive to ion cleaning energy and ion species, indicating that J_c in these devices is not controllable over a wide range. This is a problem for some cases in which control of J_c is required, such as integrated circuit applications." Further, on page 3 of *Hunt, Hunt* states that "The degraded layer on the YBCO base electrode is caused by ion damage during the edge cutting and edge cleaning steps, and presumably consists of both crystalline defects and stoichoimetry shifts associated with preferential ion sputtering." Thus, the method taught by *Hunt* results in a *degraded*, ion *damaged* layer with crystalline *defects*, and stoichiometry *shifts*, contrary to the uniform ion-modified barrier that results in the properties recited in the appealed claims.

Therefore, Applicants respectfully submit that the appealed claims are not obvious over *Harada*, in view of *Chan* and either *Hunt* or *Jia*.

SUMMARY

Applicants therefore respectfully request that the Examiner's rejection be reversed, and that all of the pending claims be allowed.

Please charge any additional fees or credit overpayment to Merchant & Gould Deposit Account No. 13-2725.

Respectfully submitted,

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PATENT TRADEMARK OFFICE
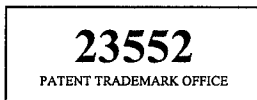
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CLAIMS APPENDIX

65.   A Josephson junction device, comprising:

a first layer comprising an oxide high-temperature superconductor;

a second layer comprising an oxide high-temperature superconductor; and

a third layer connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,

the device having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

66.   The Josephson junction device of claim 65[2], wherein the first layer comprises an YBCO superconducting oxide.

67.   An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode, having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

68.   The device of claim 67, wherein the first and second superconductive oxides are YBCO.

71.   A Josephson junction device, comprising:

a first layer comprising an oxide high-temperature superconductor;

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a second layer comprising an oxide high-temperature superconductor; and

a third layer connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,

the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

72.   The Josephson junction device of claim 71 wherein the first layer comprises an YBCO superconducting oxide.

73.   An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode,

the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

74.   The Josephson junction device of claim 73, wherein the first and second superconductive oxides are YBCO.

75.   The Josephson junction device of claim 65, wherein the third layer is substantially uniform.

EVIDENCE APPENDIX

A. OFFICE ACTIONS AND AMENDMENTS/RESPONSES

1. Advisory Action -- mailed 19 December 2008

2. Amendment under Rule 116 -- filed 5 December 2008

3. Final Office Action -- mailed 24 September 2008

4. Supplemental Amendment – filed 14 August 2008

5. Amendment – filed 28 April 2008

    a. Declaration of John M. Rowell under 37 C.F.R. 1.132

B. REFERENCES RELIED UPON BY THE EXAMINER

1. K. Harada, H. Myoren, and Y. Osaka, "Fabrication of all-high-Tc Josephson junction using as-grown $YBa_2Cu_3O_x$ thin films," Jap. J. Appl. Phys., vol. 30, pp. L1387 (1991)

2. U.S. Pat. No. 5,892,243

3. Hunt, B. *et al.,* "High Temperature Superconductor Weak Links", *Second Symposium on Low Temperature Electronics and High Temperature Superconductivity,* Electrochemical Society Meeting, Honolulu, Hawaii, Vol. 93-22, p. 467-472 (May 1993)

4. C.L. Jia *et al.,* "Effect of chemical and ion-beam etching on the atomic structure of interfaces in $YBa_2Cu_3O_7/PrBa_2Cu_3O_7$ Josephson junctions", *Appl. Phys. Lett.,* Vol 67, No. 24, 3635-3637 (1995))

RELATED PROCEEDINGS APPENDIX

None.

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.1

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,091	01/02/2004	Brian H. Moeckly	10467.43USI2	2150

23552   7590   12/19/2008
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EXAMINER
WARTALOWICZ, PAUL A

ART UNIT	PAPER NUMBER
1793	

MAIL DATE	DELIVERY MODE
12/19/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Advisory Action **Before the Filing of an Appeal Brief**	10/751,091	MOECKLY ET AL.
	Examiner	**Art Unit**	
	PAUL A. WARTALOWICZ	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED <u>05 December 2008</u> FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

   a) ☒ The period for reply expires <u>4</u> months from the mailing date of the final rejection.

   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

     Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

<u>NOTICE OF APPEAL</u>

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

<u>AMENDMENTS</u>

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will <u>not</u> be entered because

   (a)☐ They raise new issues that would require further consideration and/or search (see NOTE below);

   (b)☐ They raise the issue of new matter (see NOTE below);

   (c)☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d)☐ They present additional claims without canceling a corresponding number of finally rejected claims.

     NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: <u>65-68 and 71-75</u>.

   Claim(s) withdrawn from consideration: _____.

<u>AFFIDAVIT OR OTHER EVIDENCE</u>

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will <u>not</u> be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will <u>not</u> be entered because the affidavit or other evidence failed to overcome <u>all</u> rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

<u>REQUEST FOR RECONSIDERATION/OTHER</u>

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: <u>See Continuation Sheet.</u>

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____.

13. ☒ Other: <u>See Continuation Sheet.</u>

/Steven Bos/
Primary Examiner, Art Unit 1793

U.S. Patent and Trademark Office
PTOL-303 (Rev. 08-06)   **Advisory Action Before the Filing of an Appeal Brief**   Part of Paper No. 20081217

Continuation of 11. does NOT place the application in condition for allowance because: Applicant argues that the prior art does not teach the I_c or R_n values in the ranges in claims 65-74. However, it appears that Hunt teaches Ar ion-damaged YBCO weak link exhibiting RnA value of $2.9 * 10(-9)$ and a J_c value of $5 * 10(4)$ in Figure 2, page 9.

Continuation of 13. Other: The currently pending claims 65-68 and 71-75 are rejected under 35 USC 103(a) over Harada in view of Chan and either one of Hunt or Jia; the same as the previously rejected claims 1-5,7-21, and 59-74.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-64. (Cancelled)

65. (**Currently amended**) ~~The Josephson junction device of claim 59~~A Josephson junction device, comprising:

a first layer comprising an oxide high-temperature superconductor;

a second layer comprising an oxide high-temperature superconductor; and

a third layer connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,

the device having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

66. (**Currently amended**) The Josephson junction device of claim 65[2], wherein the first layer comprises an YBCO superconducting oxide ~~having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K~~.

67. (**Currently amended**) ~~The device of claim 1~~An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

2

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode, having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

68. (**Currently amended**)   The device of claim 67, wherein the first and second superconductive oxides are YBCO ~~having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K~~.

69. (**Cancelled**)

70. (**Cancelled**)

71. (**Currently amended**)   ~~The Josephson junction device of claim 59~~ A Josephson junction device, comprising:
    a first layer comprising an oxide high-temperature superconductor;
    a second layer comprising an oxide high-temperature superconductor; and
    a third layer connecting the first and second layers and comprising a non-superconductor,
    the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,
    the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

72. (**Currently amended**)   The Josephson junction device of claim 71 ~~62~~ wherein the first layer comprises an YBCO superconducting oxide, ~~having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K~~.

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73. (**Currently amended**)   ~~The Josephson junction device of claim 1~~<u>An electronic device comprising:</u>

<u>a crystalline substrate;</u>

<u>an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;</u>

<u>a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and</u>

<u>a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode,</u>

<u>the device</u> having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

74. (**Currently amended**)   The Josephson junction device of claim <u>73</u>[7], <u>wherein the first and second superconductive oxides are YBCO</u>~~having a Jc value of about 1×10³ to about 5×10⁶ A/cm² at 4.2K~~.

75. (**New**)   The Josephson junction device of claim 65, wherein the third layer is substantially uniform.

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.2

S/N 10/751,091   PATENT

<u>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</u>

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

EFS-Web Transmission

<u>**AMENDMENT UNDER 37 C.F.R. § 1.116**</u>

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the Office Action mailed September 24, 2008, and further in response to the Advisory Actions mailed on October 24, 2008, and December 2, 2008, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

1

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-64. (Cancelled)

65. (**Currently amended**)   ~~The Josephson junction device of claim 59~~A Josephson junction device, comprising:

a first layer comprising an oxide high-temperature superconductor;

a second layer comprising an oxide high-temperature superconductor; and

a third layer connecting the first and second layers and comprising a non-superconductor,

the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,

the device having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

66. (**Currently amended**)   The Josephson junction device of claim 6<u>5</u>[2], wherein the first layer comprises an YBCO superconducting oxide ~~having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K.~~

67. (**Currently amended**)   *~~The device of claim 1~~*An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

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a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode, having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2 K.

68. (**Currently amended**)   The device of claim 67, wherein the first and second superconductive oxides are YBCO ~~having an R_nA value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K~~.

69. (**Cancelled**)

70. (**Cancelled**)

71. (**Currently amended**)   ~~The Josephson junction device of claim 59~~ A Josephson junction device, comprising:
    a first layer comprising an oxide high-temperature superconductor;
    a second layer comprising an oxide high-temperature superconductor; and
    a third layer connecting the first and second layers and comprising a non-superconductor,
    the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer,
    the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

72. (**Currently amended**)   The Josephson junction device of claim 71 ~~62~~ wherein the first layer comprises an YBCO superconducting oxide, ~~having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K~~.

73. (**Currently amended**) ~~The Josephson junction device of claim 1~~An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode,

the device having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2 K.

74. (**Currently amended**) The Josephson junction device of claim 73[7], wherein the first and second superconductive oxides are YBCO~~having a Jc value of about 1×10³ to about 5×10⁶ A/cm² at 4.2K~~.

75. (**New**) The Josephson junction device of claim 65, wherein the third layer is substantially uniform.

Remarks

Claims 1-74 are pending, of which claims 22-58 were withdrawn. Applicants have now amended claims 65-68 and 71-74, cancelled claims 63, 64, 69 and 70 without prejudice and added claim 75. Applicants respectfully request the allowance of claims 65-76.

Substance of the Examiner Interviews

The undersigned attorney wishes to thank Examiner Wartalowicz for the telephone interviews on or about October 2, 2008 and October 28, 2008. Examiner Wartalowicz the undersigned attorney were present at both interviews.

During the interview on or about October 2, 2008, the *Jia* reference (C.L. Jia *et al.*, "Effect of chemical and ion-beam etching on the atomic structure of interfaces in $YBa_2Cu_3O_7/PrBa_2Cu_3O_7$ Josephson junctions", *Appl. Phys. Lett.*, Vol 67, No. 24, 3635-3637 (1995)) was discussed. Specifically, the nature of the $PrBa_2Cu_3O_7$ layer disclosed in the *Jia* reference was discussed. The Examiner indicated that he was willing to reconsider the significance of the *Jia* reference when a response to the Office Action was submitted.

No agreement as to the merits of the claims was reached.

During the interview on or about October 28, 2008, the Advisory Action was discussed. The Examiner confirmed that he declined to enter the Applicants' Reply submitted on October 9, 2008, not on the merits of the Applicants arguments and additions presented therein, but because certain amended and new claims presented new combinations of limitations and it was not clear to the Examiner that the amendments were adequately supported.

Explanations of the Claim Amendments and Addition

Applicants have now amended claims 65-68 and 71-74, cancelled claims 69 and 70 without prejudice and added claim 75. The details of the amendments and additions are as follows:

Claim 65 has been amended into independent form, incorporating the limitations of claim 59 of the Supplemental Amendment of August 14, 2008, except that the phrase

"substantially uniform" has been removed from "the third layer being substantially uniform".

Claim 66 has now been amended to depend on claim 65 instead of claim 62, and the limitation on the R_nA range has been replaced by the limitation of YBCO superconducting oxide for the first layer. Because claim 65 now depends on claim 59, which already includes the limitation on R_nA range, and now-cancelled claim 62 included the YBCO requirement and also ultimately depended on claim 59, the amendment to claim 66 does not introduce any new combination.

Claim 67 has been amended into independent form, incorporating the limitations of claim 1 of the Supplemental Amendment of August 14, 2008, except that the phrase "substantially uniform" has been removed from "substantially uniform barrier layer". In essence, claim 67 now incorporates the limitations of claim 1 of the Amendment filed on April 28, 2008.

Claim 68 has now been amended to depend on claim 67 instead of claim 7, and the limitation on the R_nA range has been replaced by the limitation of YBCO superconducting oxide for the first layer. Because claim 67 already includes the limitation on R_nA range, and now-cancelled claim 7 included the YBCO requirement and also ultimately depended on claim 1, the amendment to claim 68 does not introduce any new combination.

Claims 69 and 70 have been cancelled without prejudice.

Claim 71 has been amended into independent form, incorporating the limitations of claim 59 of the Supplemental Amendment of August 14, 2008, except that the phrase "substantially uniform" has been removed from "the third layer being substantially uniform". In essence, claim 71 now incorporates the limitations of claim 59 of the Amendment filed on April 28, 2008.

Claim 72 has now been amended to depend on claim 71 instead of claim 62, and the limitation on the J_c range has been replaced by the limitation of YBCO superconducting oxide for the first layer. Because claim 72 now depends on claim 71, which already includes the limitation on J_c range, and now-cancelled claim 62 included the YBCO requirement and also ultimately depended on claim 59, the amendment to claim 72 does not introduce any new combination.

Claim 73 has been amended into independent form, incorporating the limitations of claim 1 of the Supplemental Amendment of August 14, 2008, except that the phrase "substantially uniform" has been removed from "substantially uniform barrier layer". In essence, claim 73 now incorporates the limitations of claim 1 of the Amendment filed on April 28, 2008.

Claim 74 has now been amended to depend on claim 73 instead of claim 7, and the limitation on the J_c range has been replaced by the limitation of YBCO superconducting oxide for the first layer. Because claim 73 already includes the limitation on J_c range, and now-cancelled claim 7 included the YBCO requirement and also ultimately depended on claim 1, the amendment to claim 74 does not introduce any new combination.

New claim 75 depends on claim 65 and further includes the limitation that "the third layer is substantially uniform". Because claim 65 which, as explained above, has been amended into independent form, incorporating the limitations of claim 59 of the Supplemental Amendment of August 14, 2008, except that the phrase "substantially uniform" has been removed from "the third layer being substantially uniform", claim 75 is identical in scope as the version of claim 65 presented in the Supplemental Amendment of August 14, 2008. Therefore, new claim 75 does not introduce and new combination of limitations.

Applicants therefore respectfully submit that no new combination has been introduced by any claim amendment presented herein.

Claim Rejections – 35 U.S.C. § 103

Claims 1-5, 7-21 and 59-74 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30,* pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243) and either *Hunt* (Hunt, B. *et al.,* "High Temperature Superconductor Weak Links", *Second Symposium on Low Temperature Electronics and High Temperature Superconductivity,* Electrochemical Society Meeting, Honolulu, Hawaii, Vol. 93-22, p. 467-472 (May 1993)) or *Jia.* Applicants' cancellation of claims 1-64 renders the rejections of claims 1-5, 7-21 and 59-62 moot. Applicants respectfully

submit that, as previously presented, claims 65-74 contain allowable subject matter. Applicant has now amended claims 65-74 to either independent form, incorporating all limitations of any base claim and intervening claims or dependent claims based on respective non-cancelled claims without intending to surrender any claim scope as previously presented. Applicants respectfully submit that claims 65-74 are allowable as amended.

Regarding claims 65-74, or which claims 69 and 70 have now been cancelled without prejudice, the Examiner relies on *Harada* and *Jia* for the rejection. As discussed in Applicants' Amendment submitted on April 28, 2008, including the Declaration of Prof. Rowell, *Harada* does not disclose a barrier made of an ion-modified layer of a superconducting electrode. The Amendment of April 28, 2008 is incorporated herein by reference. Further, *Harada* fails to disclose or suggest the I_C or R_n values in the ranges in claims 65-74.

As to *Jia*, the Examiner contends that it discloses a substantially similar process of making the barrier layer as that of the claimed invention such that the properties of the barrier layer of *Jia* are substantially similar to the properties of the barrier layer of the claimed invention. Applicants respectfully disagree with the Examiner. *Jia* discloses a Josephson junction with a layered structure of $YBa_2Cu_3O_7/PrBa_2Cu_3O_7/YBa_2Cu_3O_7$, in which the $PrBa_2Cu_3O_7$ layer is a deposited non-superconducting barrier. *See, e.g., id* at Abstract (..."Josephson junctions formed by epitaxial $YBa_2Cu_3O_7/PrBa_2Cu_3O_7/YBa_2Cu_3O_7$ triple-layer films ...") and p. 3635, left column, first paragraph ("In most cases $PrBa_2Cu_3O_7$ is employed as nonsuperconducting barrier material.") The method disclosed in the present application and resulting in the device claimed in claims 65-74, in contrast, produces a barrier layer that is ion-modified from one of the superconductor electrodes. Therefore, the process in *Jia* is very different from that of the claimed invention such that the properties of the barrier layer of *Jia* cannot be predicted to be substantially similar to the properties of the barrier layer of the claimed invention. Moreover, in order for a device to be classified as a Josephson junction, it must display Josephson properties when measured electrically. *Jia* presents no electrical measurements, no measured values of I_c or R_n, and no evidence that the structures

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discussed operate as Josephson junctions. For at least these reasons, Applicants respectfully request the withdrawal of the rejection of claims 65-68 and 71-74.

New Claims

New claim 75 has been added. For at least the same reasons stated above, claim 75 should be allowed.

SUMMARY
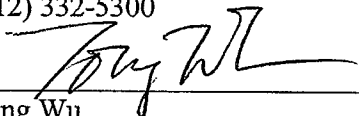
In view of the above amendments and remarks, Applicant respectfully requests a Notice of Allowance. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

Respectfully submitted,

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┌─────────────────────────┐
│        23552            │
│ PATENT TRADEMARK OFFICE │
└─────────────────────────┘
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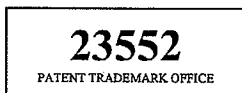
Date: <u>December 5, 2008</u>

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Tong Wu
Reg. No. 43,361
TWu/cjc

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.3

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,091	01/02/2004	Brian H. Moeckly	10467.43USI2	2150

23552   7590   09/24/2008

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER
WARTALOWICZ, PAUL A

ART UNIT	PAPER NUMBER
1793	

MAIL DATE	DELIVERY MODE
09/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/751,091	MOECKLY ET AL.
	Examiner	Art Unit	
	PAUL A. WARTALOWICZ	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2008*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-74* is/are pending in the application.

    4a) Of the above claim(s) *22-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,59-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7- 21, 59-74 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in

view of Chan (U.S. 5,892,243) and either one of Hunt et al. ("High Temperature

Superconductor Josephson Weak Links") or Jia et al. (Effect of chemical and ion-

beam...).

Figure 2 of Harada shows a Josephson junction having a crystalline substrate

MgO, a YBCO electrode formed on and epitaxial to the substrate (page 1389, column 1,

lines 4-7), an insulator a-YSZ, a barrier comprising a plasma-treated surface of the

YBCO (page 1387, column 1, second paragraph), and a YBCO counter-electrode

formed directly on and epitaxial to the barrier.

Chan teaches with respect to the cover figure to form insulator 48 epitaxially on

YBCO 46 (column 6, lines 25-32).

It would have been obvious to form an epitaxial insulator on the Harada device

instead of a-YSZ, in order to obtain the higher quality crystalline material obtained by

epitaxial growth.

With respect to claims 2-4, a process limitation carries weight in a claim drawn to

a product only when distinct structure is produced by the process. *In re Thorpe*, 227

USPQ 964 (Fed. Cir. 1985). There is no evidence of record to show that the process

steps recited would necessarily give rise to a barrier layer distinct from that of Harada.

With respect to claim 5, both of the Harada YBCO layers have their c-axis

perpendicular to the substrate (page 1389, column 1, lines 4-7). Therefor the top plane

of the lower YBCO must be an a-b plane, and a junction is formed in that plane.

With respect to the layer in-between the superconducting layers wherein the

barrier layer is produced by ion-milling the superconducting layer, Hunt teaches the

claimed process limitations (pages 3 and 4).

Jia teach forming barrier layers by ion-etching a superconductor (pg 3635, Fig 2).

Therefore, it would have been obvious to one of ordinary skill in the art to provide

a non-superconducting, ion modified surface layer of a superconducting oxide in Harada

in order to provide a barrier layer between two superconducting oxides as taught by

Hunt or Jia.

Harada et al. fail to teach the claimed I_cR_n product.

However, Hunt teach that it is known for YBCO with microbridges to exhibit an

I_cR_n product of around 1.03 mV at a temperature of 4.2 K and an I_cR_n product of around

450 μV a temperature of 77 K (pg 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time applicant's invention was made to provide the claimed I_cR_n product in Harada

because the fabrication method for making YBCO devices exhibiting the claimed I_cR_n

product are known as taught by Hunt.

With respect to claims 63 and 64, it appears that the process of making the junctions is substantially similar to the claimed invention such that the properties of the junctions of the prior art are substantially similar to those of the claimed invention.

While it appears that neither Hunt nor Jia explicitly disclose a substantially uniform ion-milled barrier layer, it appears that Hunt suggests that the Hunt teaches ion-damage barrier chips fabricated using Ar ions to etch tapered YBCO edges (page 005). it appears that Hunt treats the YBCO edge in a uniform manner.

Jia also appear to teach a substantially uniform barrier layer (pg. 3635,3636).

Therefore, it would have been obvious to one of ordinary skill in the art at the time applicant's invention was made to provide a substantially uniform barrier in Harada et al. in order to provide a barrier layer between two superconducting oxides as taught by Hunt or Jia.

As to claims 65-74, it appears that Jia teaches a substantially similar process of making the barrier layer as that of the claimed invention such that the properties of the barrier layer of Jia are substantially similar to the properties of the barrier layer of the claimed invention.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and SQUIDS").

Laibowitz et al. teaches at the bottom of column 1 of page 686 that transport along the a-b plane direction has a longer coherence length and higher current density.

It would have been obvious to arrange a junction perpendicular to the a-b plane

for these reasons. The device of Harada in figure 2 has a perpendicular portion of the

junction that would be perpendicular to the a-b plane, because the c direction is

perpendicular to the MgO substrate.

Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Harada et al. ("Fabrication of All-High-Tc Josephson Junction . . .) in

view of Chan (U.S. 5,892,243) and Laibowitz et al. ("All high T_c edge junctions and

SQUIDS") and Satoh et al. ("Effect of Lanthanum Doping of YbaCuO...").

Harada et al. fail to teach the claimed I_cR_n product.

Satoh teach a method of making YBCO (pg 1) wherein lanthanum doped YBCO

produces a higher I_cR_n product than that of pure YBCO (pp. 2, 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time applicant's invention was made to provide a higher I_cR_n product than that of pure

YBCO in Harada et al. because it is known to dope YBCO with lanthanum in order to

obtain high I_cR_n product.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to optimize an I_cR_n product, since it has been held that discovering

an optimum value or a result effective variable involved only routine skill in the art. In re

Boesch, 617 F.2nd 272, 205 USPQ 215 (CCPA 1980). The artisan would have been

motivated to optimize an I_cR_n product by the reasoning that higher I_cR_n product enables

annealing at higher temperatures for longer durations as taught by Satoh.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL A. WARTALOWICZ whose telephone number is (571)272-5957. The examiner can normally be reached on 8:30-6 M-Th and 8:30-5 on Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stanley Silverman can be reached on (571) 272-1358. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Wartalowicz
September 21, 2008   /Steven Bos/
                                                             Primary Examiner
                                                             A.U. 1793

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

ELECTRONICALLY FILED August 14, 2008

SUPPLEMENTAL AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Further to Amendment and Response filed on April 28, 2008, in response to the Office Action mailed October 26, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. **(Currently amended)** An electronic device comprising:

a crystalline substrate;

an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

a <u>substantially uniform</u> barrier comprising a non-superconducting, ion-modified surface layer of the first superconductive oxide; and

a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode.

2. (Original) The device of claim 1, wherein the barrier is a surface formed by treating the first superconductive oxide with a plasma comprising a gas selected from the group consisting of argon, xenon, oxygen, and halogen.

3. (Original) The device of claim 2, wherein the gas is argon gas.

4. (Original) The device of claim 2, wherein the gas is a 1:1 mixture of argon and oxygen.

5. (Original) The device of claim 1 wherein the first superconductive oxide has an a-b plane and a step-edge junction is formed in the a-b plane of the first superconductive oxide.

6. (Original) The device of claim 1 wherein the first superconductive oxide has an a-b plane, the a-b plane is epitaxial to the substrate, and the second superconductive

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oxide is on and epitaxial to the first superconductive element, whereby a junction is formed perpendicular to the a-b plane of the first superconductive oxide.

7. (**Currently amended**)   The device of claim[s] 1[-6], wherein the first and second superconductive oxide is YBCO.

8. (Original)   The device of claim 1, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

9. (Original)   The device of claim 2, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

10. (Original) The device of claim 3, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

11. (Original) The device of claim 4, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

12. (Original) The device of claim 5, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

13. (Original) The device of claim 6, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

14. (Original) The device of claim 7, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

15. (Original) The device of claim 1, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

16. (Original) The device of claim 2, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

17. (Original) The device of claim 3, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

18. (Original) The device of claim 4, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

19. (Original) The device of claim 5, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

20. (Original) The device of claim 6, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

21. (Original) The device of claim 7, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

22. (Withdrawn)   A process for making a Josephson junction device comprising the steps of:
    (a)   preparing a substrate;
    (b)   depositing an electrode comprising a first layer of a superconductive oxide on the substrate;
    (c)   depositing an insulating layer on the first layer of superconductive oxide;

(d)   patterning to form a pre-device having an exposed surface of the first superconductive oxide;

(e)   placing the pre-device into a deposition chamber;

(f)   forming a barrier on the exposed surface of the first layer of superconductive oxide by treating the exposed surface with plasma; and

(g)   depositing a second layer of a superconductive oxide on the pre-device, whereby a Josephson junction is formed between the first and the second superconductive oxides at the barrier.

23. (Withdrawn)   The process of claim 22, wherein the treating is with a plasma of Ar gas at a pressure of between 10 and 100 mTorr.

24. (Withdrawn)   The process of claim 22, wherein the treating is with a mixture of Ar and O_2 gas at a pressure of between 10 and 100 mTorr.

25. (Withdrawn)   The process of any one of claims 22-24, further comprising the step of vacuum annealing the pre-device prior to depositing the second superconductive oxide.

26. (Withdrawn)   A superconductor device, comprising:

a)   an oxide superconductor having a surface exposed to ambient environment; and

b)   a passivation layer covering at least a portion of the surface of the oxide superconductor that is exposed to the ambient environment.

27. (Withdrawn)   The device claim 26, further comprising a buffer layer at least partially between the passivation layer and the oxide superconductor.

28. (Withdrawn)   The device of claim 26, wherein the passivation layer originates from the superconductor.

29. (Withdrawn)   The device of claim 28, wherein the passivation layer is an ion-modified layer of the superconductor.

30. (Withdrawn)   The device of claim 26, wherein the oxide superconductor comprises $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

31. (Withdrawn)   The device of claim 26, wherein the passivation layer is an electrical insulator.

32. (Withdrawn)   The device of claim 26, wherein the passivation layer is epitaxial and crystalline.

33. (Withdrawn)   The device of claim 26, wherein the passivation layers covers the entire surface of the oxide superconductor that is exposed to the ambient environment.

34. (Withdrawn)   The device of claim 26, further comprising a layer of a superconductive oxide on the passivation layer, whereby a Josephson junction is formed between the superconductive oxides.

35. (Withdrawn)   A method of providing a passivation layer on the surface of an oxide superconductor, the method comprising vacuum annealing and plasma treating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.

36. (Withdrawn)   The method of claim 35, further comprising additional vacuum annealing after the plasma treatment.

37. (Withdrawn)   The method of claim 35, further comprising heating in an oxygen-rich environment after the plasma treatment.

38. (Withdrawn)   The method of claim 35, comprising vacuum annealing and plasma treating the entire surface of the oxide superconductor that is exposed to ambient environment

39. (Withdrawn)   A method of making a superconductor device, the method comprising:

a)   forming a layer of oxide superconductor on a substrate, the layer of oxide superconductor having a surface that is exposed to ambient environment; and

b)   passivating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.

40. (Withdrawn)   The method of claim 39, comprising passivating the entire exposed surface of the oxide superconductor.

41. (Withdrawn)   The method of claim 39, wherein the passivating step comprises bombarding the exposed surface portion with ions.

42. (Withdrawn)   The method of claim 41, further comprising annealing the layer of oxide superconductor between steps (a) and (b).

43. (Withdrawn)   The method of claim 42, further comprising annealing the layer of oxide superconductor after step (b).

44. (Withdrawn)   The method of claim 42, wherein the bombarding step comprises treating the exposed surface portion with plasma.

45. (Withdrawn)   The method of claim 39, wherein step (a) comprises forming a layer of $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

46. (Withdrawn)   The method of claim 42, further comprising heating the oxide superconductor in oxygen after step (b).

47. (Withdrawn)   The method of claim 46, further comprising cooling the oxide superconductor to room temperature in oxygen after heating the oxide superconductor in oxygen.

48. (Withdrawn)   The method of claim 41, further comprising maintaining the layer of oxide superconductor at a temperature of between about 300 0C and about 650 0C while bombarding the exposed surface portion with ions.

49. (Withdrawn)   The method of claim 46, wherein the heating step comprises maintaining the layer of oxide superconductor at a temperature of between about 700 0C and about 800 0C after treating the exposed surface portion with plasma.

50. (Withdrawn)   The method of claim 39, wherein the passivation step comprises changing a surface layer of the oxide superconductor to a material different from the oxide superconductor.

51. (Withdrawn)   The method of claim 50, wherein the changing step comprises changing the surface layer of the oxide superconductor to a material having an oxygen mobility that is lower than the oxygen mobility in the oxide superconductor.

52. (Withdrawn)   The method of claim 39, further comprising forming a layer of oxide superconductor on at least a portion of the passivated surface portion, whereby a Josephson junction is formed between the oxide superconductors.

53. (Withdrawn)   A passivation layer comprising an ion-modified layer on an oxide superconductor, the ion-modified layer covering at least a portion of the surface of the oxide superconductor that would otherwise be exposed to ambient environment, and the ion-modified layer having an oxygen mobility that is lower than an oxygen mobility of the oxide superconductor.

54. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is formed by material originating from the oxide superconductor.

55. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is an externally applied layer that is bonded to the oxide superconductor.

56. (Withdrawn)   The passivation layer of claim 55, wherein the ion-modified layer is quasi-cubic and is not $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

57. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is epitaxial and crystalline.

58. (Withdrawn)   The passivation layer of claim 53, the ion-modified layer covering the entire surface of the oxide superconductor that would otherwise be exposed to ambient environment.

59. (**Currently amended**)   A Josephson junction device, comprising:
a first layer comprising an oxide high-temperature superconductor;
a second layer comprising an oxide high-temperature superconductor; and
a third layer connecting the first and second layers and comprising a non-superconductor,
the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being a[n] substantially uniform, ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer.

60. (Previously presented)   The Josephson junction device of claim 59, wherein the first and second layers are epitaxial to each other, and wherein the third layer is formed on a ramp-edge of the first layer.

61. (Previously presented) The Josephson junction device of claim 60, further comprising a crystalline substrate supporting the first, second and third layers, wherein the first and second layers are epitaxial to the substrate.

62. (Previously presented) The Josephson junction device of claim 60, wherein the first layer comprises an YBCO superconducting oxide.

63. (Previously presented) A Josephson junction structure comprising:

a substrate; and

a plurality of Josephson junction devices of claim 1 formed on the substrate and having respective I_c values within about 7.8% of each other, and respective R_n values within about 3.5% of each other, at 4.2 K.

64. (Previously presented) The Josephson junction structure of claim 63, wherein the plurality of Josephson junctions comprise at least 10 Josephson junction devices of claim 1 and having respective I_c values within about 7.8% of each other, and respective R_n values within about 3.5% of each other, at 4.2 K.

65. (New) The Josephson junction device of claim 59, having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K.

66. (New) The Josephson junction device of claim 62, having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K.

67. (New) The device of claim 1, having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K.

68. (New) The device of claim 7, having an $R_n A$ value of about 1×10^{-9} to about 3×10^{-7} Ω-cm^2 at 4.2K.

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69. (**New**)   The device of claim 15, having an R_nA value of at least about 6×10^{-9} $\Omega\text{-cm}^2$ at 40K.

70. (**New**)   The device of claim 21, having an R_nA value of at least about 6×10^{-9} $\Omega\text{-cm}^2$ at 40K.

71. (**New**)   The Josephson junction device of claim 59, having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K.

72. (**New**)   The Josephson junction device of claim 62, having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K.

73. (**New**)   The Josephson junction device of claim 1, having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K.

74. (**New**)   The Josephson junction device of claim 7, having a J_c value of about 1×10^3 to about 5×10^6 A/cm^2 at 4.2K.

Remarks

This Supplemental Amendment is further to the Amendment and Response filed on April 28, 2008. Applicants have now amended claims 1, 7 and 59 and added claims 65-74. Applicants respectfully request the allowance of claims 1-21 and 59-74.

Substance of the Examiner Interview

The undersigned attorney and inventor Brian Moeckly wish to thank Examiner Wartalowicz for the telephone interview on June 25, 2008. Examiner Wartalowicz, Mr. Moeckly and Mr. Wu were present at the interview.

During the interview, the *Hunt* (1993) reference (Hunt, B. *et al.,* "High Temperature Superconductor Weak Links", *Second Symposium on Low Temperature Electronics and High Temperature Superconductivity,* Electrochemical Society Meeting, Honolulu, Hawaii, Vol. 93-22, p. 467-472 (May 1993)) and the obviousness rejections were discussed. Specifically, the undersigned attorney alerted the Examiner to an inadvertently erroneous characterization of the *Hunt* reference in the April 28, 2008, filing and urged the Examiner not to rely on that characterization. The undersigned attorney further stated that the *Hunt* reference did appear to disclose an ion damaged superconductor layer as a barrier between two superconductor electrodes and discussed the relevance of the *Hunt* reference.

Nature of proposed claim amendment was discussed. The Examiner indicated that claims directed to separate R_n and/or I_c could be added if adequately supported. The Examiner further indicated that claims could be amended to include the feature of uniform barrier layer.

Priority Date of the Currently Examined Subject Matter

Applicants respectfully draw the Examiner's attention to the priority date of the subject matter currently under examination. The subject matter currently under examination is disclosed in the continuation-in-part parent U.S. application 10/704,215, filed on Nov. 16, 2003, which is a continuation of U.S. application 09/082,486, filed on May 20, 1998, which claims the benefit of the U.S. provisional application 60/047,555, filed on May 22, 1997. As discussed in the Amendment and Response filed on April 28, 2008, several of the referenced cited by the Examiner are dated later than at least the

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provisional application 60/047,555 and are therefore not available as prior art to reject the relevant claims.

Claim Amendment and Addition

Applicant has now amended claims 1 and 59 to recite a "substantially uniform" ion modified barrier layer. The support for this feature can be found at least at page 11, lines 21-23, and page 13, lines 24-26. This feature is not disclosed or suggested in any cited references, including the *Hunt* reference and *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)).

Claim 7 was amended to eliminate its multi-dependency.

New claims 65-74 have been added to recite R_nA and J_c values of the claimed devices. The support for the amendments can be found at least at page 13, lines 4-18, and Figure 6 in the drawings. These values are not disclosed or suggested in the cited references relating to Josephson junctions with ion-damaged barriers. *Hunt*, for example, discloses an R_nA value of only 5×10^{-10} Ω-cm^2 for junctions made of ion-damaged layer. *See, Hunt* at page 007. As discussed at least at page 4, lines 25-29 of the Specification, junctions with low R_nA values imply high J_c values for usefully high I_cR_n products, and the J_c in relevant prior art devices is typically too high for applications such as single flux quantum (SFQ) logic devices. For example, *Hunt* discloses a J_c of 5.5×10^6 A/cm^2 and states that a "potential problem is that the device current densities are approaching the electrode J_c values." *See, Hunt* at page 006. That is, J_c values are too high, and the junction is not a weak link at all. In contrast, the claimed devices possess high R_nA values and correspondingly low J_c values, such as 5×10^6 A/cm^2 or lower.

Applicants therefore respectfully submit that the claims are patentable over the cited prior art.

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SUMMARY

In view of the above amendments and remarks, Applicant respectfully requests a Notice of Allowance. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

23552
PATENT TRADEMARK OFFICE

Respectfully submitted,

MERCHANT & GOULD P.C.
P.O. Box 2903
Minneapolis, Minnesota 55402-0903
(612) 332-5300

Date: August 14, 2008

/Tong Wu/
Tong Wu
Reg. No. 43,361
TWu:rlk

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

AMENDMENT AND RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the Office Action mailed October 26, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 11 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. **(Currently amended)**   An electronic device comprising:

(a)——a crystalline substrate;

(b)——an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;

(c)——an insulator formed on and epitaxial to the electrode;

(d)——a barrier comprising a non-superconducting, ion-modified plasma-treated surface layer of the first superconductive oxide; and

(e)——a counter-electrode formed directly on and epitaxial to the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode.

2. (Original)   The device of claim 1, wherein the barrier is a surface formed by treating the first superconductive oxide with a plasma comprising a gas selected from the group consisting of argon, xenon, oxygen, and halogen.

3. (Original)   The device of claim 2, wherein the gas is argon gas.

4. (Original)   The device of claim 2, wherein the gas is a 1:1 mixture of argon and oxygen.

5. (Original)   The device of claim 1 wherein the first superconductive oxide has an a-b plane and a step-edge junction is formed in the a-b plane of the first superconductive oxide.

6. (Original)   The device of claim 1 wherein the first superconductive oxide has an a-b plane, the a-b plane is epitaxial to the substrate, and the second superconductive

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oxide is on and epitaxial to the first superconductive element, whereby a junction is formed perpendicular to the a-b plane of the first superconductive oxide.

7. (Original)   The device of any one of claims 1-6, wherein the first and second superconductive oxide is YBCO.

8. (Original)   The device of claim 1, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

9. (Original)   The device of claim 2, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

10. (Original) The device of claim 3, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

11. (Original) The device of claim 4, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

12. (Original) The device of claim 5, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

13. (Original) The device of claim 6, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

14. (Original) The device of claim 7, the device having an I_cR_n value of at least about 0.3 mV at a temperature of 4.2 K.

15. (Original) The device of claim 1, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

16. (Original) The device of claim 2, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

17. (Original) The device of claim 3, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

18. (Original) The device of claim 4, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

19. (Original) The device of claim 5, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

20. (Original) The device of claim 6, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

21. (Original) The device of claim 7, the device having an I_cR_n value of at least about 0.5 mV at a temperature of 40 K.

22. (Withdrawn)   A process for making a Josephson junction device comprising the steps of:

(a)   preparing a substrate;

(b)   depositing an electrode comprising a first layer of a superconductive oxide on the substrate;

(c)   depositing an insulating layer on the first layer of superconductive oxide;

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(d)   patterning to form a pre-device having an exposed surface of the first superconductive oxide;

(e)   placing the pre-device into a deposition chamber;

(f)   forming a barrier on the exposed surface of the first layer of superconductive oxide by treating the exposed surface with plasma; and

(g)   depositing a second layer of a superconductive oxide on the pre-device, whereby a Josephson junction is formed between the first and the second superconductive oxides at the barrier.

23. (Withdrawn)   The process of claim 22, wherein the treating is with a plasma of Ar gas at a pressure of between 10 and 100 mTorr.

24. (Withdrawn)   The process of claim 22, wherein the treating is with a mixture of Ar and O_2 gas at a pressure of between 10 and 100 mTorr.

25. (Withdrawn)   The process of any one of claims 22-24, further comprising the step of vacuum annealing the pre-device prior to depositing the second superconductive oxide.

26. (Withdrawn)   A superconductor device, comprising:

a)   an oxide superconductor having a surface exposed to ambient environment; and

b)   a passivation layer covering at least a portion of the surface of the oxide superconductor that is exposed to the ambient environment.

27. (Withdrawn)   The device claim 26, further comprising a buffer layer at least partially between the passivation layer and the oxide superconductor.

28. (Withdrawn)   The device of claim 26, wherein the passivation layer originates from the superconductor.

29. (Withdrawn)   The device of claim 28, wherein the passivation layer is an ion-modified layer of the superconductor.

30. (Withdrawn)   The device of claim 26, wherein the oxide superconductor comprises $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

31. (Withdrawn)   The device of claim 26, wherein the passivation layer is an electrical insulator.

32. (Withdrawn)   The device of claim 26, wherein the passivation layer is epitaxial and crystalline.

33. (Withdrawn)   The device of claim 26, wherein the passivation layers covers the entire surface of the oxide superconductor that is exposed to the ambient environment.

34. (Withdrawn)   The device of claim 26, further comprising a layer of a superconductive oxide on the passivation layer, whereby a Josephson junction is formed between the superconductive oxides.

35. (Withdrawn)   A method of providing a passivation layer on the surface of an oxide superconductor, the method comprising vacuum annealing and plasma treating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.

36. (Withdrawn)   The method of claim 35, further comprising additional vacuum annealing after the plasma treatment.

37. (Withdrawn)   The method of claim 35, further comprising heating in an oxygen-rich environment after the plasma treatment.

38. (Withdrawn)   The method of claim 35, comprising vacuum annealing and plasma treating the entire surface of the oxide superconductor that is exposed to ambient environment

39. (Withdrawn)   A method of making a superconductor device, the method comprising:

a)   forming a layer of oxide superconductor on a substrate, the layer of oxide superconductor having a surface that is exposed to ambient environment; and

b)   passivating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.

40. (Withdrawn)   The method of claim 39, comprising passivating the entire exposed surface of the oxide superconductor.

41. (Withdrawn)   The method of claim 39, wherein the passivating step comprises bombarding the exposed surface portion with ions.

42. (Withdrawn)   The method of claim 41, further comprising annealing the layer of oxide superconductor between steps (a) and (b).

43. (Withdrawn)   The method of claim 42, further comprising annealing the layer of oxide superconductor after step (b).

44. (Withdrawn)   The method of claim 42, wherein the bombarding step comprises treating the exposed surface portion with plasma.

45. (Withdrawn)   The method of claim 39, wherein step (a) comprises forming a layer of $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

46. (Withdrawn)   The method of claim 42, further comprising heating the oxide superconductor in oxygen after step (b).

47. (Withdrawn)   The method of claim 46, further comprising cooling the oxide superconductor to room temperature in oxygen after heating the oxide superconductor in oxygen.

48. (Withdrawn)   The method of claim 41, further comprising maintaining the layer of oxide superconductor at a temperature of between about 300 °C and about 650 °C while bombarding the exposed surface portion with ions.

49. (Withdrawn)   The method of claim 46, wherein the heating step comprises maintaining the layer of oxide superconductor at a temperature of between about 700 °C and about 800 °C after treating the exposed surface portion with plasma.

50. (Withdrawn)   The method of claim 39, wherein the passivation step comprises changing a surface layer of the oxide superconductor to a material different from the oxide superconductor.

51. (Withdrawn)   The method of claim 50, wherein the changing step comprises changing the surface layer of the oxide superconductor to a material having an oxygen mobility that is lower than the oxygen mobility in the oxide superconductor.

52. (Withdrawn)   The method of claim 39, further comprising forming a layer of oxide superconductor on at least a portion of the passivated surface portion, whereby a Josephson junction is formed between the oxide superconductors.

53. (Withdrawn)   A passivation layer comprising an ion-modified layer on an oxide superconductor, the ion-modified layer covering at least a portion of the surface of the oxide superconductor that would otherwise be exposed to ambient environment, and the ion-modified layer having an oxygen mobility that is lower than an oxygen mobility of the oxide superconductor.

54. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is formed by material originating from the oxide superconductor.

55. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is an externally applied layer that is bonded to the oxide superconductor.

56. (Withdrawn)   The passivation layer of claim 55, wherein the ion-modified layer is quasi-cubic and is not $YBa_2Cu_3O_{7-\delta}$, wherein $\delta \geq 0$.

57. (Withdrawn)   The passivation layer of claim 53, wherein the ion-modified layer is epitaxial and crystalline.

58. (Withdrawn)   The passivation layer of claim 53, the ion-modified layer covering the entire surface of the oxide superconductor that would otherwise be exposed to ambient environment.

59. (New)   A Josephson junction device, comprising:
a first layer comprising an oxide high-temperature superconductor;
a second layer comprising an oxide high-temperature superconductor; and
a third layer connecting the first and second layers and comprising a non-superconductor,
the first and third layers being formed from a starting oxide high-temperature superconductor layer of an oxide high-temperature superconductor, the third layer being an ion-modified portion of the starting oxide high-temperature superconductor layer, the first layer being an unmodified portion of the starting oxide high-temperature superconductor layer.

60. (New)   The Josephson junction device of claim 59, wherein the first and second layers are epitaxial to each other, and wherein the third layer is formed on a ramp-edge of the first layer.

61. (New)   The Josephson junction device of claim 60, further comprising a crystalline substrate supporting the first, second and third layers, wherein the first and second layers are epitaxial to the substrate.

62. (New)   The Josephson junction device of claim 60, wherein the first layer comprises an YBCO superconducting oxide.

63. (New)   A Josephson junction structure comprising:
    a substrate; and
    a plurality of Josephson junction devices of claim 1 formed on the substrate and having respective I_c values within about 7.8% of each other, and respective R_n values within about 3.5% of each other, at 4.2 K.

64. (New)   The Josephson junction structure of claim 63, wherein the plurality of Josephson junctions comprise at least 10 Josephson junction devices of claim 1 and having respective I_c values within about 7.8% of each other, and respective R_n values within about 3.5% of each other, at 4.2 K.

Remarks

Claims 1-58 are pending, of which claims 22-58 have been withdrawn from consideration, and claims 1-21 have been rejected. Applicants have amended claim 1 and added claims 59-64 without introducing any new matter, and respectfully request the allowance of claims 1-21 and 59-64.

Claim Rejections under 35 U.S.C. § 103

Claims 1-5 and 7 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243). Applicants have amended claim 1 and respectfully submit that claims 1-5 and 7 are allowable.

The present application relates to an Interface-Engineered Josephson Junction ("IEJ"), in which the barrier layer is formed by modifying a surface layer of a superconductor electrode, rather than depositing a non-superconducting layer on the electrode. Claim 1 includes, among other things, the features that the barrier between the superconducting electrodes comprises "a non-superconducting, ion-modified surface layer of the first superconductive oxide" and that the counterelectrode is epitaxial to the barrier. Both *Harada* and *Chan* fail to disclose or suggest these features.

Applicants had distinguished the claimed invention from *Harada* in view of *Chan* in several responses to Office Actions in U.S. Patent Application Serial Number 09/082,486 (the "'486 application), which is a parent application to the present application. The responses include: (1) Response filed on July 13, 2001, in response to the Office Action mailed on March 13, 2001; Response filed on December 11, 2001 (entered with the Request for Continued Examination filed on March 8, 2002), in response to the Final Rejection mailed on October 11, 2001; and (3) Response filed on January 2, 2003, in response to the Office Action mailed July 2, 2002. For brevity, Applicants will not restate those arguments here in their entirety, but instead incorporate those arguments herein by reference and highlight the following: Neither *Harada* nor *Chan* discloses or suggests a barrier that is an ion-modified layer of superconductive oxide electrode. In fact, instead of forming a non-superconducting barrier by ion-

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modification of the superconductive electrode, the purpose of the plasma processing in *Harada* is to <u>remove</u> contaminants and other nonsuperconducting phase. *See,* page L1388. Any epitaxial relationship between the electrode and counterelectrode in the structure disclosed in *Harada* is due to the fact that they were both grown on the same single crystalline MgO substrate. *See,* page L1388.

Applicants further submit herewith the Declaration of John M. Rowell under 37 C.F.R. 1.132. Professor Rowell is an expert in the relevant technology. As the National Academy of Science notes in its citation, Prof. Rowell "is known for his contributions to the basic understanding and applications of superconductivity: the first observation of the Josephson effect; the quantitative verification of the electron-phonon interaction as the mechanism responsible for conventional superconductivity; and the translation of these accomplishments to applications of both low and high Tc superconductors." (*See,* National Academy of Science Member Directory, accessible at http://www.nasonline.org/site/Dir/1959908160?pg=vprof&mbr=1004919&returl=http%3 A%2F%2Fwww.nasonline.org%2Fsite%2FDir%2F1959908160%3Fpg%3Dsrch%26vie w%3Dbasic&retmk=search_again_link.)

As Prof. Rowell notes in his Declaration, it is not clear from *Harada* that a barrier made of an ion-modified surface layer of a high-T_c superconductor was produced. The conclusion is due at least to (a) poor Josephson junction reported by *Harada,* (b) the ambiguous statements made in *Harada* regarding the plasma treatment, and (c) *Harada*'s report of using the lift-off technique to expose the surface to be treated by plasma. Furthermore, simply experimenting with the process reported by *Harada* paper would not have lead to the Josephson junction disclosed and claimed in the present application.

Furthermore, regarding *Chan,* it only discloses a ***deposited*** barrier. *See, e.g.,* col. 8, lines 3-11 of *Chan. Chan* therefore teaches away from the claimed invention and cannot be properly combined with *Harada.*

The cited references therefore do not render obvious claims 1-5 and 7.

The non-obviousness the claims are further demonstrated by the fact that the invention disclosed and claimed in the present application is widely recognized as being the first successful IEJ. The embodiments of the invention disclosed in the present application is also described in the publication, B.H. Moeckly and K. Char, "Properties of

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interface-engineered high T_c Josephson junctions", *Appl. Phys. Lett.* 71(17), pp., 2526-2528 (1997) (the "Moeckly/Char paper"). To date, over 160 papers, over 150 of which by authors other than either of the Applicants, have cited the Moeckly/Char paper. Several of those papers are attached herewith as examples of statements people have made about the Moeckly/Char paper. The attached papers include:

1. T. Satoh, *et al.*, "Effect of lanthanum doping of YBaCuO electrode's on the characteristics of modified-interface edge junctions", *IEEE Transactions On Applied Superconductivity*, 13(2) pp. 791-793 (2003) ("Interface modification has been investigated as a process for fabricating highly uniform barriers, instead of barrier deposition or growth, for high-temperature superconducting (HTS) Josephson junctions. Moeckly and Char [1] were the first to demonstrate a reliable fabrication process for such junctions." (citing the Moeckly/Char paper.))

2. J. Yoshida, *et al.*, "Interfacce-Engineered Junctions with HbBACuO as the Counter-Electrode", *IEEE Transactions On Applied Superconductivity*, 13(2) pp. 599-602 (2003) ("Interface-engineered junctions (IEJs) are regarded as the most promising candidates for high-T_c digital circuit applications as they are superior to other high-T_c Josephson junctions in terms of uniformity and reproducibility [1]-[3]." (citing the Moeckly/Char paper and two other papers published later than the effective filing date of the present application.)

3. J. Yoshida, *et al.*, "Current transport in interface-engineered high-T_c Josephson junctions", *Physica C*, 367, pp. 260-266 (2002) ("The basic concept of an IEJ is to create a this barrier layer by altering the structure or chemistry of the base-electrode layer only at the surfaces [1]" (citing the Moeckly/Char paper.))

4. H. Katsuno, *et al.*, "Characteristics of interface-engineered Josephson junctions using a $YbBa_2Cu_3O_y$ counterelectrode layer", *Appl. Phys. Lett.*, 79(25), pp. 4189-4191 (2001) ("The interface-engineering technique proposed by Moeckly and Char[1] is regarded as the most promising method for fabricating high-temperature superconductor Josephson junctions for digital circuit application because of the resultant high uniformity in junction characteristics." (citing the Moeckly/Char paper.))

5. J. Kye, *et al.*, "Interface-modified YBCO ramp-edge Josephson junctions by deionized water", *Supercond. Sci. Technol.*, 14, pp. 1056-1059 (2001) ("Several years ago Moeckly and Char fabricated interface-modified ramp-edge type HTSC JJ without depositing any artificial barrier [1]" (citing the Moeckly/Char paper.))

6. Tinchev, *et al.* "Interface-engineered' high-T-c Josephson junctions: a possible mechanism of operation", *Supercond. Sci. Technol.*, 12, pp. L5-L7 (1999) ("Ramp-type Josephson junctions fabricated without any deposited interlayer

and in which the barrier is created by an interface modification have attracted great attention recently [1-4]." (citing the Moeckly/Char paper and three other papers published later than the effective filing date of the present application.))

7. Y. Wu, *et al.,* "Structural variation of the interface-engineered layers in $YBa_2Cu_3O_{7-\delta}$ thin films", *Physica C,* 366, pp. 51-56 (2002) ("Recently, Moeckly et al. have developed an interface-engineered junction (IEJ), in which no barrier deposition is involved [5, 6]." (citing the Moeckly/Char paper and another paper by Moeckly and Char and published later than the effective filing date of the present application.))

8. J. K. Heinsohn *et al.,* "Current transport in ramp-type junctions with engineered interface", *J. Appl. Phys.,* 89(7), pp. 3852-3860 (2001) ("The idea of fabricating a barrier by interface treatments instead of using an epitaxially grown nonsuperconducting thin film was first suggested by Moeckly *et al.*[1]" (citing the Moeckly/Char paper.))

9. J. Yoshida, "Recent progress of high-temperature superconductor Josephson junction technology for digital circuit applications", *IEICE Trans. Electron.,* E83-C(1), pp. 49-59 (2000) ("A completely new approach to create an artificial barrier layer in ramp-edge-type junctions without the deposition of any barrier materials has recently been demonstrated by Moeckly and Char [10]." (citing the Moeckly/Char paper.))

10. J. G. Wen, *et al.,* "Atomic structure and composition of the barrier in the modified interface high-T_c Josephson junction studied by transmission electron microscopy", *Appl. Phys. Lett.,* 75(16), pp. 2470-2472 (1999) ("Recently, interface-engineered $YBa_2Cu_3O_y$ (YBCO) junctions (IEJ), developed by Moeckly *et al.*[1,2] attracted much attention since the reproducible and manufacturable process of fabrication is quite suitable for digital circuit applications." (citing the Moeckly/Char paper and another yet-unpublished paper.))

Claims 1-5 and 7 are therefore allowable over *Harada* and *Chan.*

Claims 6 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30,* pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243), further in view of *Laibowitz* ("All high T_c edge junctions and SQUIDS"). Applicants respectfully traverse.

As discussed above, *Harada* in view of *Chan* does not render claim 1 obvious. *Laibowitz* does not supply what is missing in this regard. Therefore, the cited three references do not render claim 1 obvious, and therefore do not render claim 6 obvious.

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Claims 8-12, 14-19 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243) and any of *Hunt (1993), Ishimaru (2002), Kito (2002) and the Moeckly/Char paper.* Applicants respectfully traverse.

First, Applicants respectfully notes that *Ishimaru, Kito* and the *Moeckly/Char paper* were published after the effective filing date of the present application with respect to the elected claims and therefore are not available as prior art references. Second, with respect to *Hunt,* as discussed above, *Harada* in view of *Chan* does not render claim 1 obvious. *Hunt* does not supply what is missing in this regard. Therefore, the cited three references do not render claim 1 obvious, and therefore do not render any of claims 8-12, 14-19 and 21 obvious.

It should be particularly pointed out that claims 8-21 had been deemed to contain allowable subject matter in the '486 application, which is a parent application to the present application (claims 8-21 are numbered 12-25, respectively, in the '486 application.) *See,* Office Actions mailed on July 2, 2002, and May 6, 2003 (the latter, while stating that claims 12-25 are rejected, does not set forth any ground for the rejection.) The Examiner cites *Hunt* and the three non-prior art references to support the disclosure of various I_cR_n product values. However, of the only reference available as prior art, *Hunt* discloses only a deposited barrier. *See,* the "Device Fabrication" section of *Hunt.* It therefore teaches away from the claimed invention and should not be combined with *Harada* and *Chan* as basis for claim rejection.

Claims 8-12, 14-19 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243) and *Satoh (2002).* Applicants respectfully traverse. Applicants respectfully notes that *Satoh* was published after the effective filing date of the present application with respect to the elected claims and therefore are not available as prior art references.

Claims 13 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-

grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243) and *Laibowitz,* and further in view of any of *Hunt (1993), Ishimaru (2002), Kito (2002) and the Moeckly/Char paper.* Applicants respectfully traverse. As discussed above, *Harada, Chan and Laibowitz* fail to render claim 1 obvious. Further, *Ishimaru, Kito* and the *Moeckly/Char paper* were published after the effective filing date of the present application with respect to the elected claims and therefore are not available as prior art references. Further, *Hunt* teaches away from the claimed invention because it discloses a deposited barrier. Claims 13 and 20 are therefore not obvious over the cited references.

Further as noted above, claims 13 and 20 had been previously deemed to contain allowable subject matter in the parent '486 application and should be now allowed.

Claims 13 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Harada* ("Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991)) in view of *Chan* (U.S. 5,892,243) and *Laibowitz,* and further in view of *Satoh (2002).* Applicants respectfully traverse. As discussed above, *Satoh* was published after the effective filing date of the present application with respect to the elected claims and therefore are not available as prior art references.

Applicants therefore respectfully request the allowance of claims 1-21.

New Claims

New claims 59-64 have been added. For at least the same reasons set forth above for the allowability of claims 1-21, Applicants respectfully request the allowance of claims 59-64.
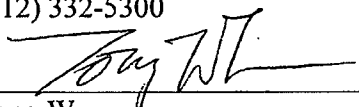
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SUMMARY

In view of the above amendments and remarks, Applicant respectfully requests a Notice of Allowance. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

23552
PATENT TRADEMARK OFFICE

Respectfully submitted,

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Date: <u>April 28, 2008</u>

Tong Wu
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Properties of interface-engineered high T_c Josephson junctions

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We have created YBCO thin film ramp edge Josephson junctions by modification of the edge surface prior to counterelectrode deposition. No deposited interlayer or barrier layer is employed. These devices are uniform and reproducible, and they display resistively shunted junction current-voltage characteristics with excellent magnetic field modulation. $I_c R_n$ values over the range 0.5–3 mV and corresponding $R_n A$ values of 6×10^{-8}–1.2×10^{-9} Ω cm^2 at 20 K are easily attained by varying the process. We believe these junctions offer significant promise as the building blocks of a high T_c electronics technology. © *1997 American Institute of Physics.*
[S0003-6951(97)02443-1]

Successful implementation of a high T_c circuit technology based on Josephson devices requires the reproducible fabrication of junctions with appropriate values of key electrical properties as well as a suitably small spread of these parameters. It appears essential to have nonhysteretic critical currents (I_cs) in the range 100–500 μA, normal resistance (R_n) values of one to several ohms, and inductances of several pH, with 1 σ spreads in I_c less than 10% for a minimum of 100 junctions. Other important requirements are the ability to operate in a reasonable temperature range (10–77 K) and the capability of flexible junction placement on the circuit chip. In addition, a slow, nonexponential variation of $I_c(T)$ is desirable in order to increase the temperature range of operation and reduce the spread in I_c. Thus far, simultaneous satisfaction of these requirements has proven elusive.

The two looming difficulties of the S/interlayer/S devices are control of the S/interlayer interface and control of the structural and electrical properties of the interlayer. In most high T_c superconductor-normal-superconductor (SNS)-type junctions made to date, R_n of the device is clearly inconsistent with the value of resistivity of the interlayer. It has been shown that this excess resistance occurs at the interface[1] and most likely arises from oxygen sublattice disorder[2,3] caused by thermal and lattice-expansion mismatches. For the case of doped YBCO barriers,[4,5] however, the excess interface resistance has been reduced to less than 10^{-10} Ω cm^2, leading to observation of what may be a true proximity effect device. Indeed, YBCO edge junctions based on Co–YBCO barriers represent the state of the art in terms of reproducibility and uniformity.[6,7] However, the Co–YBCO junctions made at Conductus have the drawback of intrinsically low values of R_n (typically a fraction of an ohm), which demands high values of J_c for a useful $I_c R_n$ product. A high-resistivity barrier material is thus required. Unfortunately, the ability to controllably deposit lattice-matched, high-resistivity, pinhole-free layers on the scale of a few nm (the barrier thickness must decrease with increasing barrier resistivity) is presently beyond our capability and would demand significant advances in our materials science knowledge of these compounds.

We have thus pursued an approach to edge junction formation based on the *elimination of a deposited interlayer.* We believe this will alleviate complications related to deposition of doped-YBCO materials.[8] Drawing on lessons learned from elimination of problems at the S/interlayer interface,[1,9] in the present work, we used the interfacial properties *to our advantage.* Different phases of YBCO have vastly different electrical properties. In loose analogy with the oxidation process used in low T_c tunnel junctions,[10] our goal was to reliably modify, either chemically or structurally, the exposed YBCO edge prior to deposition of the YBCO counterelectrode, thereby forming a type of *intrinsic* barrier free of the problems of deposited layers and complex compounds. This idea was catalyzed by the results of experiments we undertook to anneal YBCO films, which showed that the whole of an orthorhombic film could be easily converted to a cubic phase simply by appropriate low-temperature vacuum annealing.[11] We have also recently become aware of and encouraged by work which has indicated that ion plasma treated YBCO surfaces may lead to Josephson behavior.[12] Other work has also shown that a thin layer of cubic PBCO could be formed on the surface of an orthorhombic PBCO film by ion milling.[13] We also note that all-YBCO junctions have been previously produced by depositing a (perhaps cubic) YBCO interlayer at low temperatures, but these devices have been difficult to reproduce[14] or have displayed poor Josephson characteristics.[15]

Our intent is to provide only the surface of YBCO with enough kinetic energy to convert it to a different phase or structure, leaving the rest of the film in the orthorhombic state. We speculate that creation of the interlayer involves the rearrangement of Y and Ba atoms in such a way as to destroy their long-range translational order, thereby forming a quasi-cubic phase. Such a structure has been observed for YBCO films grown at low temperature.[16]

To create the engineered interface, we employ an *in situ* plasma treatment prior to deposition of the YBCO counterelectrode, as follows. The YBCO ramp edge is formed by our usual Ar ion milling procedure.[4] Immediately prior to surface treatment and deposition of the top YBCO counterelectrode, the baselayer is given an Ar ion mill clean at 500 V. The sample is then mounted in the laser deposition chamber and heated to between 400 and 600 °C in vacuum for 30 min. Next we form a plasma by biasing the heater with an rf source, using Ar and/or O$_2$ as the ionizing gas at pressures of
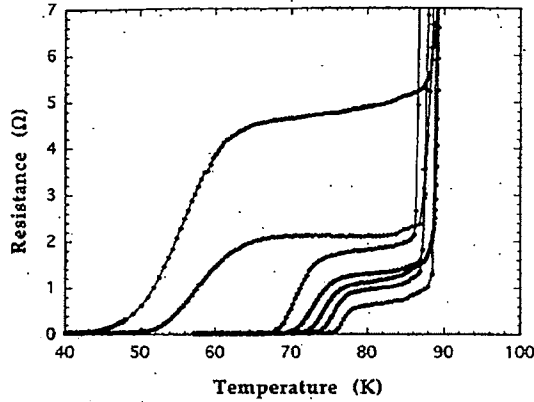
[a]Electronic mail: moeckly@conductus.com

FIG. 1. The resistance vs temperature for several interface-engineered junctions with different values of R_n.
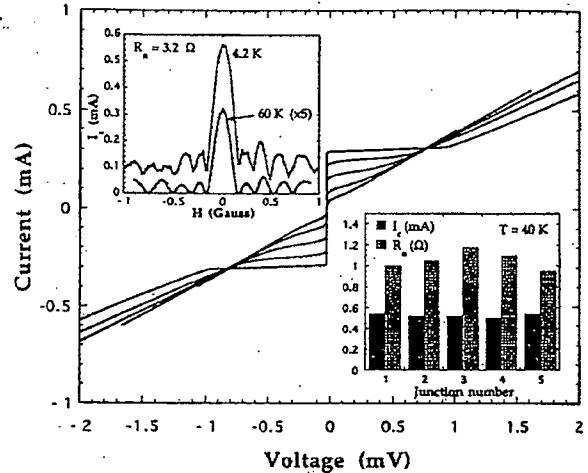

FIG. 2. Examples of the RSJ-like I-V characteristics of a single junction at 4.2, 20, 30, 40, and 50 K. The insets show the magnetic field modulation of I_c for a different junction (the field is applied perpendicular to the plane of the substrate; note that the edge of the junctions is actually at an angle to this surface) and values of I_c and R_n obtained at 40 K for junctions on one of our test chips. The junction dimensions are 4 μm $\times$ 150 nm.

10–100 mTorr. We perform this plasma treatment for several minutes with a forward power of 100–400 W and a dc self-bias of 200–900 V. Values of the gas pressures and rf power are selected to determine the junction parameters. Following the plasma treatment, an optional further vacuum annealing step may be performed. The second YBCO layer is then deposited in the usual manner under our standard conditions. Last, these multilayered films are patterned to form five junctions per chip with cross-sectional dimensions of 4 μm by 150 nm (the thickness of the base YBCO).

Upon cooling below the transition temperature T_c of the YBCO leads, we observe for these devices a well-defined resistance from the sharp transition at T_c down to the onset of the detectable junction critical current which occurs at a lower temperature, T_0. Figure 1 displays this behavior for several different junctions. These data indicate that the altered interface layer appears to be well localized; we observe no smeared transition or long "tail" to the superconducting state. Note that the temperature T_0 varies inversely as the value of the junction resistance above T_0. This resistance is approximately equal to the value of the junction resistance R_n determined from the resistively shunted junction (RSJ)-like current-voltage (I-V) characteristics below T_0. There is also a clear inverse scaling relationship between R_n and I_c. We note that the dependence of T_0 on R_n is much stronger than that for high-angle grain-boundary weak link junctions, which have a similar magnitude of $R_n A$. Our observed relationship may imply a different transport mechanism (or certainly a "barrier" with different properties) than that which governs high T_c grain boundaries. Electron-beam damaged junctions[17–19] actually exhibit a stronger relationship than ours, although their values of $R_n A$ and $I_c R_n$ are far lower, and they operate only over a much narrower temperature range. (Also, our junctions are completely stable at room temperature.)

Below the temperature T_0 at which a critical current appears, we see I-V characteristics described by the RSJ model; we have observed such I-Vs on each completed device of the over 350 we have measured. These RSJ-like I-Vs are also observed over a wide range of tunable junction parameters; for example, at 40 K, $I_c R_n$ is adjustable between

0.1 and 2 mV at present. Examples of the I-V characteristics for a single junction at several temperatures are shown in Fig. 2. At high temperatures we often observe zero excess current and 100% magnetic field modulation (see below); at lower temperatures excess current often appears, consistent with the onset of the wide junction limit $w > 4\lambda_J$. However, when J_c is sufficiently small, RSJ-like behavior persists over the entire temperature range from T_0 to 4.2 K. At low temperatures we sometimes observe slight hysteresis at the onset to the nonzero-voltage state. This can be attributed to a significant McCumber parameter β_c due to a high R_n rather than to an inordinately large junction capacitance. For junction resistances R_n of many ohms, we find that the I-Vs become nonlinear at high voltage bias. We have also observed this effect in high-resistance Co–YBCO grain-boundary junctions.[11] Thus the quasiparticle transport giving rise to R_n is not strictly metallic.

This fact is clear from the behavior of R_n with temperature. As seen in Fig. 3(a), the junction resistance tends to increase with decreasing T for R_n greater than a couple of ohms. Thus whatever the material giving rise to the resistance in our junctions is, it appears to be near some sort of metal–insulator transition. The nature of Josephson transport in this regime is not well understood, although we speculate that the existence of localized states plays a dominant role in the conduction process of these devices.

As shown in Fig. 3(b), we observe the familiar quasi-linear dependence of I_c on T as seen for most types of high T_c weak links except the Co–YBCO and Ca–YBCO SNS-type junctions[5,20] in which a clear exponential behavior is observed. We do not believe this behavior clarifies the nature of the weak-link effect in our junctions, and we cannot conclude that they are either "shorts" or "proximity effect" devices. In addition, we have not carefully measured $I_c(T)$ near T_0 by taking noise rounding into account, because this behavior is intrinsically nondefinitive.
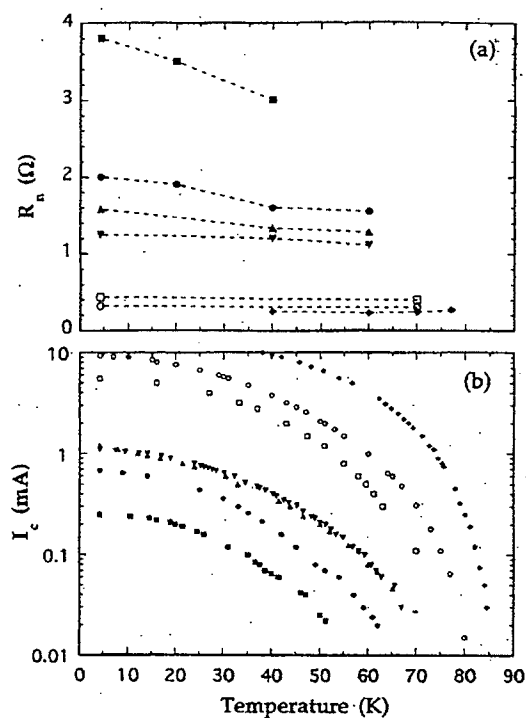
FIG. 3. Dependence of (a) R_n and (b) corresponding I_c on temperature for several different junctions.

In the inset of Fig. 2 we present an example of the behavior of I_c in a magnetic field for a 3 Ω junction at two temperatures; a Fraunhofer-like diffraction pattern is observed. I_c is suppressed completely to zero at high temperatures and still modulates by nearly 80% at 4.2 K. The period of the $I_c(H)$ modulation of $\sim$0.2 G correlates satisfactorily to the physical junction width of 4 μm if flux focusing is taken into account.[21]

In order for these devices to be useful in multi-junction circuits, junction-to-junction uniformity is required and, indeed, remains the primary hurdle to implementation of high T_c circuit technology. We believe our elimination of a deposited barrier layer will avoid many problems associated with nonuniformities. Our evaluation of over 70 five-junction test chips has demonstrated initial uniformities better than any junction technology previously pursued at Conductus. An example of the spread in I_c and R_n over five such junctions is shown in the lower inset of Fig. 2.

Finally, we mention that these junctions thus far appear to be quite stable. Their I_c and R_n values do not change over a period of several months' storage in atmosphere. Furthermore, we have annealed a 0.5 Ω junction chip in oxygen at 400 °C for 10 h and found that the junction parameters remain constant. These junctions even survive a high-temperature anneal at the growth temperature of 785 °C in 400 mTorr O_2 for 30 min: subsequent measurements revealed excellent RSJ behavior with a decrease of R_n and increase of J_c by about a factor of 2. Since cations begin to move at this high temperature, this result is not surprising, and we are encouraged by the fact that the junctions appear to be robust under conditions that would be used, for ex-

ample, in the subsequent deposition of ground planes, insulators, or interconnects.

To summarize, we have demonstrated a method of fabricating all-YBCO high T_c edge Josephson junctions which intentionally avoids the deposition of a barrier layer. These devices appear to be uniform and reproducible, and their electrical characteristics are easily adjustable within a range which is useful for electronic circuits. For example, an I_c of several hundred μA and an R_n of 2 Ω at 40 K is ideally suited for single flux quantum technology. We note that uniformity of these ramp edge junctions may be approaching the limit achievable in this geometry (we have already measured 1 σ spreads in I_c lower than 8% for 10 junctions), so we deem it prudent to investigate the utility of this technique in a trilayer geometry. Finally, we stress that these junctions directly demonstrate that control of the interfaces in high T_c multilayer device technology is of paramount importance. Due to the complex nature of YBCO, deposited barrier layers of other materials in an SNS geometry are not required to achieve reliable junction operation. We believe that the properties of many SNS-type high T_c junctions are in fact dominated by the Josephson effect at the (perhaps not well-controlled) interfaces.

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B. H. Moeckly and K. Char

Effect of Lanthanum Doping of YBaCuO Electrodes on the Characteristics of Modified-Interface Edge Junctions

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Abstract—With the aim of improving the interface-modification process—a standard technique for forming the barrier in high-temperature superconducting Josephson junctions, lanthanum doping of a YBaCuO electrode was successfully attempted in this study. Accordingly, it was confirmed that lanthanum doping significantly affects junction characteristics; that is, it produces a lower critical current density and higher normal state resistance. In other words, lanthanum doping increased the annealing temperature or time for the barrier-formation process. These effects are advantageous for the growth of the counter layer, and for high-temperature processes made after the junction fabrication, such as upper-layer groundplane integration. It was confirmed that the lanthanum doping of the base electrode has a significant effect on the junction characteristics. It was also found that the lanthanum doping produces benefits in terms of higher critical current and normal-state resistance product.

Index Terms—Fabrication, high-temperature superconductors, Josephson junctions, surface treatment.

I. INTRODUCTION

INTERFACE modification has been investigated as a process for fabricating highly uniform barriers, instead of barrier deposition or growth, for high-temperature superconducting (HTS) Josephson junctions. Moeckly and Char [1] were the first to demonstrate a reliable fabrication process for such junctions. In their fabrication process for "interface-engineered junctions" (IEJ's), the barrier was formed on the surface of a base $YBa_2Cu_3O_{7-\delta}$ (YBaCuO) electrode of an edge junction by structurally modifying YBaCuO by using an argon and/or oxygen plasma treatment and vacuum annealing. The IEJ's showed resistively and capacitively shunted junction (RCSJ)-like current-voltage ($I–V$) characteristics and excellent uniformity of critical current (I_c).

Satoh *et al.* [2], [3] reported a similar kind of uniform barrier-formation process, which included amorphization by ion irradiation and crystallization by oxygen annealing, and demonstrated the possibility of larger-scale integration of modified-interface edge junctions. They showed that I_c spreads (1σ) were as small as 8% for 100 edge junctions.

Recently, Soutome *et al.* [4] reported I_c spreads (1σ) as small as 7.9% for 100 modified-interface edge junctions with integrated groundplanes. Other researchers also reported uniform junction characteristics [5], [6] for this kind of junction. Today, this interface-modification technique has been established as one of the most reliable barrier-formation methods for HTS Josephson junctions. It has also been studied as a fabrication process for HTS trilayer junctions [7], [8].

To improve junction characteristics and uniformity, the fabrication process of the modified-interface barrier must be further studied. For example, to maintain a barrier thickness for good junction characteristics, a growth temperature of the counter YBaCuO layer, namely the annealing temperature of the barrier, is sometimes limited to lower temperature than the appropriate values. The low growth temperature may cause incomplete epitaxial growth, or inferior superconducting properties of YBaCuO films. For making higher temperature range available for the annealing process, we were interested in a lanthanum doping of the YBaCuO electrode.

Solubility, superconducting critical temperature (T_c), and lattice parameter of lanthanum-doped YBaCuO (La-YBaCuO) material have been studied previously [9], [10]. The maximization of T_c to 97–99 K for lanthanum doping with x of 0.05 to 0.07 was reported [9], [10]. Motivated by the higher T_c of La-YBaCuO than that of YBaCuO, Hunt *et al.* [11] used La-YBaCuO as a material for the superconducting electrodes of edge junctions. Hunt *et al.* [12] also found that a-axis grain formation was able to be eliminated, that normal state resistance (R_n) was able to be increased, and that critical current density (J_c) of edge junction was able to be lowered by lanthanum doping of a YBaCuO electrode. We also studied such effects on parameters in the barrier-formation process, in particular the annealing temperature or duration of the barrier. Other researchers [13], [14] also used and studied lanthanum-doped YBaCuO electrodes for edge junctions.

This paper describes our experimental results on effects of the lanthanum doping of a YBaCuO electrode on junction characteristics and on the processing parameters of modified-interface junctions. It is confirmed that the doping increases the annealing temperature and time for the barrier-formation process. The doping effect of the base electrode on junction characteristics was confirmed. It was also found that lanthanum-doped YBaCuO produces a higher I_cR_n product than that of pure YBaCuO.
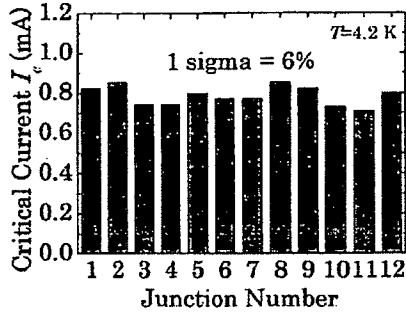
Fig. 1. Critical current (I_c) uniformity at 4.2 K for 12 modified-interface junctions with MgO as a substrate and CeO$_2$ as an insulator layer. Both electrodes were made with pure YBaCuO. The 1σ spread was 6% at 4.2 K.

II. FABRICATION PROCESS

Lanthanum-doped YBaCuO films, pure YBaCuO films, and insulator films were grown by KrF pulsed laser deposition. High-density Y(Ba$_{2-x}$La$_x$)Cu$_3$O$_{7\pm\delta}$ targets were used for the lanthanum-doped YBaCuO growth, where x = 0.025, 0.05, or 0.10. Four kinds of junctions—with counter/base electrode combinations of YBaCuO/YBaCuO (Y/Y), YBaCuO/ La-YBaCuO (Y/LY), La-YBaCuO/YBaCuO (LY/Y), or La-YBaCuO/ La-YBaCuO (LY/LY)—were fabricated.

Modified-interface barriers were conventionally fabricated by forming a surface amorphous layer by argon-ion irradiation and crystallizing it by oxygen annealing. In the annealing process, the samples were first heated for about 25 min, during which the sample temperature rose from room temperature to the annealing temperature (T_{ann}), and additionally heated at this temperature for an annealing duration (t_{ann}). A counter layer was then deposited on the sample at this temperature. The full details of the fabrication process for the modified-interface junctions are given elsewhere [2], [3].

Low-dielectric constant materials, such as MgO, are usually used as substrates, and CeO$_2$ is usually used as an insulator layer. We previously confirmed that modified-interface junctions with the same RCSJ-like junction characteristics as those of previous works [2], [3], and with highly uniform characteristics, were able to be fabricated from these materials. Fig. 1 shows the uniformity in I_c of these junctions, in which both the base and the counter electrodes consist of pure YBaCuO. The uniformity (1σ) in I_c was 6% for 12 junctions.

III. RESULTS AND DISCUSSION

First we fabricated all four kinds of junctions (Y/Y, Y/LY, LY/Y, and LY/LY) by using La-YBaCuO with x of 0.05 in order to study the doping effect on junction characteristics. The annealing process parameters were the same for all samples; i.e., T_{ann} = 760°C and t_{ann} = 3 min.

Fig. 2 shows J_c for these four different kinds of junctions. It is clear that J_c decreases while R_n increases by lanthanum doping of the YBaCuO electrode, as stated in previous reports [12], [14]. This effect was observed both for the doping of the counter electrode and the doping of the base electrode. However, the change in J_c for the junction doped at the base electrode is
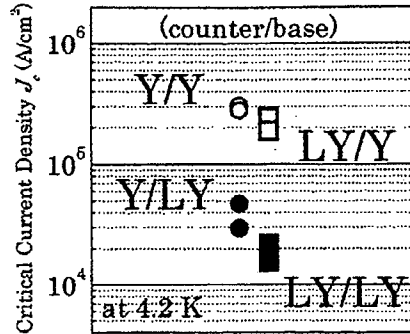
Fig. 2. Critical current density (J_c) at 4.2 K of modified-interface junctions. Open (closed) symbols: nondoped (lanthanum doped) base electrode. Circle (square) symbols: nondoped (lanthanum doped) counter electrode. For all lanthanum-doped YBaCuO, lanthanum content x was 0.05. For all samples, annealing process parameters were same; i.e., T_{ann} = 760°C and t_{ann} = 3 min.

larger than that for the junction doped at the counter electrode. The previous studies [12], [14] also pointed out the importance of the doping of the base electrode.

These measurements suggest that the presence of lanthanum during the barrier-formation process, which includes amorphization and crystallization, plays an essential role in the change in junction characteristics. Because of the small amount of lanthanum, it is unlikely that the doping will affect the amorphization. The doped lanthanum and possibly diffused lanthanum from the base electrode presumably affects the barrier-crystallization process. Lanthanum diffusion from the counter electrode to the barrier may occur and may affect the junction characteristics, but this effect is not dominant.

The dependence of the doping effect on lanthanum composition was also studied. Non-doped junctions (Y/Y), and lanthanum-doped junctions (LY/LY) with x of 0.025, 0.05, or 0.10 were fabricated under the same annealing temperature, T_{ann}, of 760°C and various annealing durations, t_{ann}. As shown in Fig. 3, J_c of junctions processed under the same annealing condition continuously decreases with increasing amount of lanthanum doping. This effect appears to saturate x of 0.05.

In addition, Fig. 3 shows the dependence of J_c on t_{ann}. The critical current density J_c for all junctions depends exponentially on t_{ann}, and does not saturate. The slopes for all junctions, namely, the rate of J_c increase during the annealing, are nearly the same. It can thus be that lanthanum doping only shifts the curves; it does not change their slope.

In other words, lanthanum doping enabled higher T_{ann} or longer t_{ann} in the annealing process for the same J_c. In our experiment, the lanthanum doping with x of 0.05 enabled about 50°C higher T_{ann} for the same t_{ann}, or about 6 min longer t_{ann} for the same T_{ann}. These are advantageous for the fabrication process of HTS integrated circuits, for example, the growth of the counter layer, and high-temperature processes made after the junction fabrication, such as upper-layer groundplane integration.

To reveal how lanthanum doping affects the barrier properties, we analyzed the junction parameters. For example, we
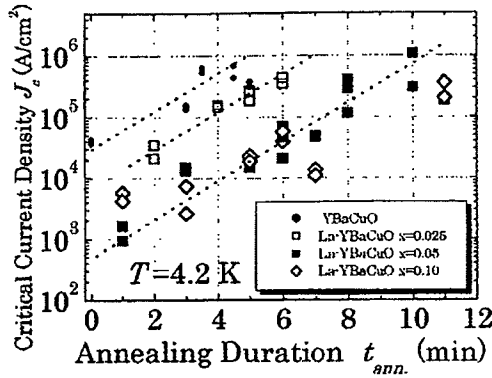
Fig. 3. Dependence of critical current density (J_c) at 4.2 K on the annealing duration t_{ann}. For YBaCuO junctions (closed circle), pure YBaCuO was used for both the base and the counter electrode. For lanthanum-doped YBaCuO junctions, $Y(Ba_{2-x}La_x)Cu_3O_{7\pm\delta}$ was used for both the base and the counter electrode, but lanthanum content (x) was different; 0.025 (open square), 0.05 (closed square), or 0.10 (open diamond) for each junction. Annealing temperature was the same for all samples; i.e., $T_{ann} = 760°C$. The dotted lines are just guides for the eye.

TABLE I
COMPARISON OF JUNCTION PARAMETERS

Electrode	$YBa_2Cu_3O_{7-\delta}$	$Y(Ba_{2-x}La_x)Cu_3O_{7\pm\delta}$
I_c	14 µA	15 µA
R_n	33 Ω	62 Ω
I_cR_n	0.46 mV	0.93 mV
β_c	1	1.7
C	19 fF	9.7 fF
d/ε_r	1.1 nm	2.2 nm

compared two junctions, which have nearly the same I_c but were processed different conditions; namely, T_{ann} of 720°C for the nondoped junction (Y/Y), T_{ann} of 760°C for the lanthanum-doped junction (LY/LY). Estimated junction parameters were summarized in Table I. The normal state resistance of the doped junction (R_n) is twice that of the nondoped junction; consequently, the I_cR_n product is as twice as large. This high I_cR_n product is one of the advantages of lanthanum doping.

We estimated the McCumber parameter (β_c) from hysteresis of the I–V curves for the junctions described above. Parameters β_c, I_c, and R_n were used to calculate capacitance of junction (C), and the ratio of barrier thickness to relative dielectric constant (d/ε_r). In spite of higher T_{ann} for the lanthanum-doped junction, I_c is the same as that of the pure YBaCuO junction, but the barrier thickness for the lanthanum-doped junction is larger, if ε_r is unchanged by the doping.

As described above, the lanthanum doping presumably affects the barrier crystallization process. The estimated junction parameters suggest that the lanthanum doping suppresses the decrease in the barrier thickness during the crystallization process.

IV. SUMMARY

We studied lanthanum doping of a YBaCuO electrode with the aim of improving the fabrication process of modified-interface junctions. It was confirmed that lanthanum doping affects junction characteristics in terms of lower J_c and higher R_n. In other words, regarding the barrier-formation process, lanthanum doping enabled annealing at higher temperature or for longer duration. These are two advantageous for the growth of the counter layer and for the high-temperature processes, such as upper-layer groundplane integration, performed after junction fabrication. It was confirmed that the doping of the base electrode has a significant effect on junction characteristics. Moreover, it was found that the higher I_cR_n product is a benefit of the lanthanum doping for the switching speed of the junctions.

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Interface-Engineered Junctions With YbBaCuO as the Counter-Electrode

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Abstract—The electric properties of interface-engineered junctions with $YbBa_2Cu_3O_7$ as the counter-electrode were investigated. The junctions exhibited excellent Josephson characteristics with the critical current density (J_c) ranging from 10^2 A/cm^2 to more than 10^6 A/cm^2, and the normal resistance (R_n) ranging from 10^{-6} Ωcm^2 to 10^{-9} Ωcm^2. The R_n values varied approximately in accordance with J_c^{-p}, where p was close to 0.25 for low-J_c junctions and increased gradually up to 0.75 for high-J_c junctions. The junctions with R_n exceeding 10^{-7} Ωcm^2 exhibited dI/dV profiles peculiar to tunneling processes via localized states. The dI/dV profiles of the junctions with lower R_n were characterized by reproducible fine structures below 15 mV, probably due to multiple Andreev reflections. These results indicate that the crossover from the tunneling regime to metallic weak-links takes place in these junctions depending on the process conditions.

Index Terms—Andreev reflection, interface-engineered junction, Josephson junction, tunneling.

I. INTRODUCTION

INTERFACE-ENGINEERED junctions (IEJ's) are regarded as the most promising candidates for high-T_c digital circuit applications as they are superior to other high-T_c Josephson junctions in terms of uniformity and reproducibility [1]–[3]. However, the electrical properties of IEJ's are sensitive to the substrate temperature for the counter-electrode deposition, and the I_c value appropriate for single flux quantum (SFQ) circuits can be obtained only in a low substrate temperature range. This temperature range sometimes conflicts with the requirement for the complete c-axis orientated growth of the counter-electrode layer with minimum sheet inductance L_s, especially when sputter-deposited $YBa_2Cu_3O_7$ (YBCO) is utilized as the counter electrode.

Recently, we reported that this trade-off between I_c and L_s could be solved by adopting $YbBa_2Cu_3O_7$ (YbBCO) as the counter-electrode, because it can grow with complete c-axis orientation in a far wider temperature range than is possible with other 123 compounds [3]. Those junctions with a completely c-axis-oriented YbBCO counter electrode exhibited excellent Josephson characteristics with the 1 σ-spread in I_c of 5.4% for 16 junctions with an average I_c of around 1 mA at 4.2 K.

In spite of such progress in the fabrication technology, neither the structure of the barrier nor the current transport mechanism in IEJ's is well understood. Reliable experimental data on the current transport in IEJ's is highly desired not only for promoting the understanding of the junction physics but also to find a way to further reduce the 1σ-spreads in I_c values.

II. FABRICATION PROCESS

IEJ's with YbBCO as the counter-electrode were fabricated on ramp-edges formed in 200-nm thick YBCO base-electrode layers. An epitaxial $SrTiO_3$, CeO_2, or $SrSnO_3$ film was used for the interlayer isolation. We have not observed any significant difference in junction characteristics among junctions with different isolation layers. All the films used in the present work were grown on $SrTiO_3$ (100) substrates using an off-axis sputtering system.

Ramp-edge structures were produced using a photoresist mask reflowed after patterning, together with Ar-ion milling with substrate rotation during etching. The resultant ramp edges had a taper of 20 degrees independent of the edge orientation in a wafer. After etching, the samples were heated to the temperature for the subsequent layer deposition and maintained at that temperature for 10 minutes. An activated oxygen flux from an ECR plasma source was supplied during this annealing process. Then, a 300-nm thick YbBCO layer was deposited and the counter-electrode pattern was formed after covering the wafer surface with a 1-μm thick Au film. The junction width was fixed at 4 μm throughout the present work.

Empirically, we know that the junction characteristics are sensitive to the substrate temperature for the counter-electrode deposition and the power supplied to the ECR plasma source during the annealing process. Other factors that have significant influence on the junction characteristics are the acceleration voltage and the incident angle of the Ar-ion beam utilized for the fabrication of the ramp-edge structure. By varying these process parameters, we have obtained IEJ's with a Josephson critical current density (J_c) ranging from 10^2 to 10^6 A/cm^2. From among the large number of junctions, only those exhibiting excellent Josephson characteristics with a magnetic field modulation of I_c exceeding 75% at 4.2 K were selected for detailed investigation.

III. JUNCTION CHARACTERISTICS

Fig. 1 depicts an example of the current-voltage $(I–V)$ characteristics observed at 4.2 K for an IEJ with a critical current density amounting to 4.5×10^5 A/cm^2. The pale line represents the $I–V$ curve in a magnetic field of 7.4×10^3 A/m applied parallel to the junction interface. It is apparent that the $I–V$ charac-
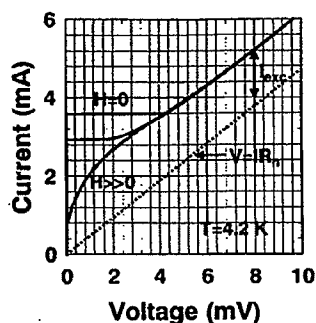
Fig. 1. Current-voltage characteristics observed at 4.2 K for an IEJ with a J_c of 4.5 × 10⁵ A/cm² with and without an applied magnetic field which minimizes the zero-voltage current. The broken line represents simple ohmic behavior for reference.
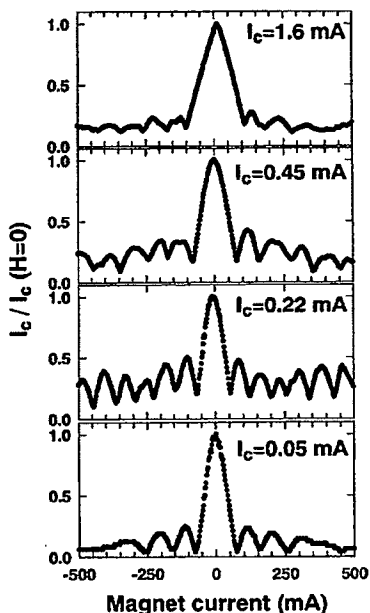
Fig. 2. Magnetic modulation of I_c observed for IEJ's with various Josephson critical currents. The crossover from small junction behavior to large junction behavior is seen between I_c = 0.5 mA and 1 mA.

Fig. 3. Correlation between R_n and I_c observed for IEJ's processed under various conditions. R_n varies approximately in accordance with I_c^{-p} with p ranging from 0.25 to 0.75 depending on I_c. Variation in R_n with a factor of 3–4 is seen for junctions with similar I_c values in the high I_c region.
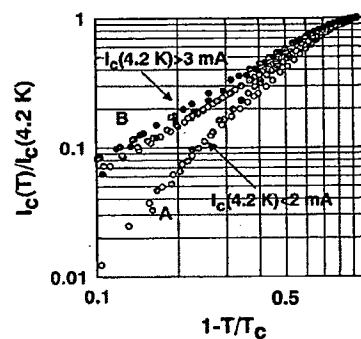
Fig. 4. Normalized I_c versus temperature characteristics for several junctions with different I_c values. The temperature dependence can be classified into two groups with an I_c at 4.2 K of 2–3 mA as the borderline.

teristics contain a large amount of excess current (I_{exc}) at high voltages. The excess current grows rapidly within an approximate voltage range of less than 5 mV, being accompanied by a weak bump-like structure within this voltage range. We also found that I_{exc}/I_c varied approximately in proportion to I_c for junctions with I_c exceeding 0.5 mA, and amounted to 30% for a junction with I_c ~ 7 mA. Such behavior seems to be consistent with the observation by Sydow et al. for their ozone-annealed IEJ's [4]. All these experimental results indicate that the excess current is not entirely due to the flux-flow behavior of the accidental microshorts in the junction but has close relation to Josephson characteristics.

Fig. 2 shows the magnetic field dependences of I_c observed at 4.2 K. The magnetic field modulation of I_c is almost 100% for low-I_c junctions, and is more than 80% even for a junction with I_c far exceeding 1 mA. In Fig. 2, we can see the crossover

from a small junction behavior to a large junction one by increasing the I_c value. The crossover takes place at I_c between 0.5 mA and 1 mA, which seems to be consistent with the London penetration depth of around 0.2 μm in high-T_c superconductors at 4.2 K.

Fig. 3 displays the correlation between the junction resistance (R_n) and I_c obtained for junctions on various wafers processed under various conditions. We defined the R_n value as the differential resistance within a current level of two to three times I_c. It can be seen that R_n varies approximately in accordance with I_c^{-p}, where p is close to 0.25 for junctions with an extremely small I_c value and is about 0.75 for junctions with I_c > 1 mA.

Another interesting point we can see in Fig. 3 is the large variation in R_n for junctions with similar I_c in the high I_c region. If we look at the junctions with I_c of 1 mA, we notice that the R_n value ranges from 1.3 to 5 Ω. Such variation in R_n is certainly beyond any experimental error, and suggests that the critical factors that influence I_c and R_n are not completely identical.

Fig. 4 shows the temperature dependences of I_c observed for several junctions with different I_c and R_n values. We found that the I_c versus temperature characteristics of our junctions could be classified into two groups with an I_c of 2–3 mA at 4.2 K as the borderline. Junctions with I_c smaller than 2 mA are characterized by their $(1 - T/T_c)^2$ dependence near T_c, as shown by
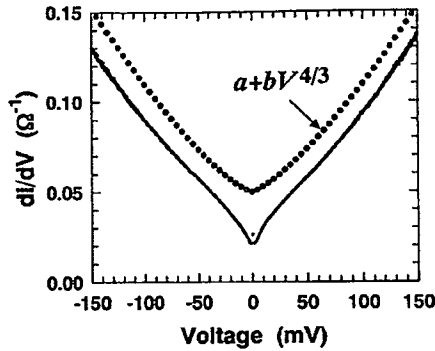
Fig. 5. Differential conductance versus Voltage characteristics at 4.2 K observed for an IEJ with I_c of 0.03 mA and R_n of 40 Ω at 4.2 K. The dotted line represents $V^{4/3}$ dependence for reference.

Fig. 6. Differential conductance versus voltage characteristics observed for an IEJ with an R_n of around 10 Ω.

group A. On the other hand, junctions with an I_c exceeding 3 mA exhibited nearly $(1 - T/T_c)^{3/2}$ dependence (group B). It is known that Josephson junctions with thin normal conducting or reduced-T_c layers on both sides of a rigid interface barrier with low transparency exhibit $(1 - T/T_c)^2$ dependence, and this dependence changes to $(1 - T/T_c)^{3/2}$ when the normal conducting layer on one side of the interface disappears [5]. Such a picture seems to be consistent with our experimental data.

Fig. 5 shows the differential conductance versus voltage $(dI/dV - V)$ characteristics observed for an IEJ with an I_c of 0.03 mA and an R_n of 40 Ω at 4.2 K. The dI/dV profile can be characterized by a slightly nonlinear increase in the conductance at high voltages, and a symmetrical dip structure around zero voltage. We found that the nonlinear behavior at high voltages was essentially independent of temperature, and fit well by $V^{4/3}$, as shown by the dotted line in the figure. This indicates that inelastic tunneling via two localized states in the barrier plays a part in the quasiparticle transport at high voltages [6]. IEJ's with R_n far exceeding 10 Ω exhibited similar characteristics. Thus, it seems reasonable to think that IEJ's with a high normal resistance have an insulator barrier with a high density of localized states in it.

It is well recognized that, in tunnel junctions with a barrier containing localized states, resonant tunneling through the localized states often dominates the quasiparticle transport at low voltages, while Cooper pairs can transfer only by direct tunneling [7]. The existence of different transport channels for quasiparticles and Cooper pairs manifests itself in the different tunnel barrier thickness dependences of I_c and R_n, resulting in a peculiar relationship between I_c and R_n as R_n is proportional to I_c^{-p} with p of less than 1. In the case where the quasiparticle current is dominated entirely by resonant tunneling, p is 0.5. This value becomes smaller when a contribution from inelastic processes via more than two localized states becomes noticeable. Generally, inelastic tunneling via n localized states is known to give $p = (n + 1)^{-1}$, and the relative importance of inelastic processes increases as the tunnel barrier thickness increases [6]. Thus, we can expect a gradual decrease in p with an increase in the junction resistance. This is exactly what we saw in Fig. 3 for our IEJ's with R_n far larger than 10 Ω.
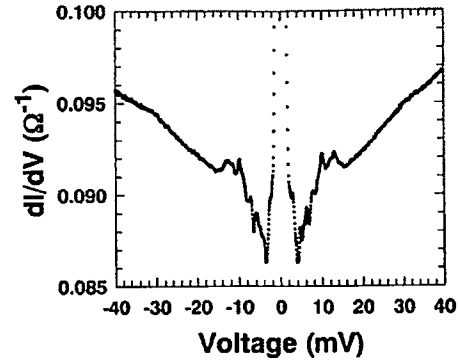
The origin of the symmetrical dip around zero voltage is not clear at present. A possible explanation may be an off-site Coulomb charging energy in the resonant tunneling process [8].

The dI/dV profiles of IEJ's having an R_n of around 10 Ω or less differ considerably from those of higher-resistance junctions. Fig. 6 depicts the dI/dV profile at 4.2 K observed for a junction with an R_n of slightly larger than 10 Ω. We can see distinct fine structures in the profile below 15 mV, and also some anomaly around 30 mV. We confirmed that the structures, at least those below 15 mV, were reproducible among junctions, and were enhanced with decreasing R_n. We also noticed that the sharpness of the fine structures correlated with the I_c value of individual junctions, i.e., when we compared two junctions with similar R_n values, the junction with the higher I_c always exhibited more pronounced structures in its dI/dV profile. Another feature we found in our low-R_n junctions is that the differential conductance of junctions with an R_n of several ohms or higher increases as the voltage increases, while that of junctions with R_n of a few ohms shows the opposite behavior.

The seemingly intricate experimental data mentioned above can be understood by assuming two kinds of current transport channels coexisting in the junctions. We think that one of them carries the Josephson current, and is also responsible for the weak bump-like structure in $I-V$ characteristics in magnetic fields, the fine structures in dI/dV profiles, and the negative coefficient of dI/dV versus V in high bias regions. Another channel is a resistive one which gives rise to a positive curvature in dI/dV versus V characteristics. This channel has little effect on the Josephson current other than providing a shunting resistor within a junction. If we assume that the relative dominance of these two transport channels varies with process conditions, we can then systematically explain the wide variety of junction characteristics observed for our IEJ's.

It has long been recognized that some superconducting microbridges exhibit peculiar characteristics similar to those of the first transport channel in the IEJ's we described above [9]. Klapwijk, Blonder, and Tinkham first pointed out the importance of the multiple Andreev reflection (MAR) process in such junctions, and demonstrated that the singularities in dI/dV profiles below the gap voltage (subharmonic gap structure, SGS) as well as the excess current at high voltages were the consequences of the MAR process [10].

The MAR process manifests itself most clearly as singularities in dI/dV profiles at voltages $V_n = 2\Delta/en$, $n = 1, 2, 3, \ldots$, where Δ is the superconducting gap of the junction electrodes. Unfortunately, the fine structures below 15 mV in our junctions shown in Fig. 6 do not permit such simple labeling of the singularities. Moreover, in most cases, we were not able to find reproducible structures at higher voltages, though the junction shown in Fig. 6 exhibits an exceptionally weak anomaly around 30 mV. Similar deviation from the simple MAR model has been reported for the singularities in dI/dV profiles of ramp-edge junctions with a PrBaCuO barrier [11]. In this case, the absence of regular periodicity in SGS has been ascribed to the existence of a reduced-T_c layer adjacent to the tunnel barrier. The presence of such reduced-T_c layers was confirmed for our IEJ's through the temperature dependence of I_c. According to the recent theoretical investigations, the proximity effect between the reduced-T_c layer and the superconducting electrode also smears out the SGS singularity at $V = 2\Delta/e$ [12], [13]. All these facts seem to support the picture that the singularities in the dI/dV profiles of our IEJ's originate from the MAR process.

It is natural to suppose that the resonant tunneling of quasiparticles via localized states in an insulative barrier, which is similar to that in high-resistance junctions, constitutes the resistive channel even in low-resistance junctions. We suppose that the tunneling region exists dispersively in the junction area without forming a continuous barrier in such junctions exhibiting the MAR process. The relative area occupied by the tunneling channel as well as the resonant tunneling probability of quasiparticles would vary with process conditions, resulting in a variation in R_n by a factor of 3–4 even for junctions with similar I_c values.

IV. SUMMARY

We have shown experimental evidence of two different transport channels in interface-engineered junctions, of which the relative dominance varies with the process conditions. We confirmed that elastic and inelastic tunneling via localized states embedded in an insulator dominate the quasiparticle transport in junctions with R_n far exceeding 10^{-7} Ωcm^2, indicating that these junctions are essentially tunnel junctions. Although we do not have concrete evidence, it seems rational to think that direct tunneling of Cooper pairs through the barrier is responsible for the Josephson current in these junctions.

The situation of junctions with a lower R_n is more complicated. We confirmed that these junctions exhibited a substantial amount of excess currents as well as peculiar singularities in their dI/dV profiles, indicating that MAR plays a significant role. The presence of normal conducting or reduced-T_c layers adjacent to the junction interface and parallel conduction through tunneling paths similar to those in higher-R_n junctions was also inferred from experiments. These results indicate that IEJ's with a high J_c and a low R_n, and thus of particular importance for SFQ circuit applications, are inhomogeneous in terms of their microscopic structures. At present, we do not have sufficient data to discuss to what extent this inherent inhomogeneity in junction structure restricts the achievable minimum 1σ-spread in I_c. Further detailed investigations are definitely required to answer this question.

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Current transport in interface-engineered high-T_c Josephson junctions

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Abstract

The mechanisms of current transport in interface-engineered junctions (IEJs) were investigated based on more than 400 junctions fabricated under various process conditions. We confirmed that the $I_c R_n$ values of IEJs scaled with the square root of the Josephson critical current density (J_c) universally, as long as the junctions had a low critical current density of less than 1×10^4 A/cm^2 at 4.2 K. These low-J_c junctions exhibited dI/dV profiles peculiar to inelastic tunneling via two or less localized states with some remnant of a smeared superconducting gap. In contrast, we could not observe a universal scaling relation between $I_c R_n$ and J_c among higher-J_c junctions. The maximum $I_c R_n$ values of IEJs having J_c ranging from 10^4 to 10^6 A/cm^2 were limited to 2–3 mV at 4.2 K. The dI/dV profiles of these high-J_c junctions differed considerably from those of low-J_c junctions, and were characterized by a highly smeared-out superconducting gap with a reproducible sub-gap structure. The differential conductance at high bias voltages increased slightly with decreasing temperature. These results indicate that a simple tunneling picture is inadequate to describe IEJs with high-J_c values. © 2002 Elsevier Science B.V. All rights reserved.

1. Introduction

Interface-engineered junctions (IEJs) are regarded as the most promising candidates for the construction of high-T_c digital circuits because they are superior to other high-T_c Josephson junctions in terms of uniformity and reproducibility. The basic concept of an IEJ is to create a thin barrier layer by altering the structure or chemistry of the base-electrode layer only at the surfaces [1]. Even a conventional ion-milling process to form a ramp-edge structure in base electrodes followed by a counter-electrode deposition in an appropriate condition was confirmed to be sufficient to form an interface barrier for Josephson junctions [2]. The spread in the Josephson critical current (I_c) of this type of junction was reported to be as low as 6.6% for a 100-junction array [3], and was 10% even for 1000 junctions [2].

The structure and the chemical composition of the barrier at the interface as well as the current transport mechanism in the junctions, however, are still the subject of intensive investigations. Although transmission electron microscopy stud-

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ies have revealed a well-crystallized material with pseudo-cubic symmetry of around 2–3 nm in thickness continuously covering the ramp-edge surface, at least for IEJs with a relatively low Josephson critical current density (J_c) [4,5], such a barrier seems to disappear in high-J_c junctions [3]. These results indicate that the structure of the interface barrier may be process dependent. Therefore, there is a possibility that various current transport mechanisms coexist within the junction, and the relative importance of the individual mechanism depends on the fabrication process. In fact, some authors have already pointed out that resonant tunneling of quasiparticles plays an important role in low-J_c junctions while a metallic channel dominates the Josephson current in high-J_c junctions [6,7].

In this paper, we report an intensive study of the current transport mechanisms in IEJs based on more than 400 junctions we have fabricated so far, under various process conditions.

2. Junction fabrication

IEJs with either $YBa_2Cu_3O_{7-x}$ (YBCO) or $YbBa_2Cu_3O_{7-x}$ (YbBCO) as the counter-electrode material were fabricated on ramp edges formed in YBCO base-electrode layers. An epitaxial $SrTiO_3$ or CeO_2 film was used for the interlayer isolation. All the films used in the present work were grown on $SrTiO_3$(1 0 0) substrates using an off-axis sputtering system. The advantage of YbBCO as the counter-electrode material compared with the conventional YBCO lies in the fact that it can grow with complete c-axis orientation in a far wider temperature range than is possible with other 123 compounds [8]. This enables us to investigate the dependence of the junction characteristics on the substrate temperature for the counter-electrode deposition in a wide range without sacrificing the quality of the counter-electrode layer. Details of our thin-film growth technique have been published elsewhere [6,9].

Ramp-edge structures were produced using a photoresist mask reflowed after patterning, together with Ar-ion milling with substrate rotation during etching. The resultant ramp edges had a
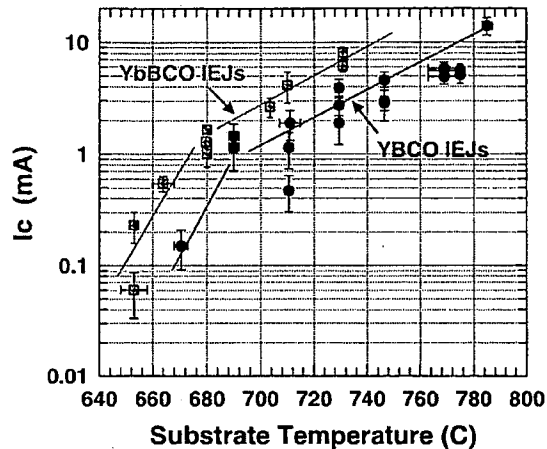
Fig. 1. Critical current at 4.2 K averaged over 16 junctions in a chip versus substrate temperature obtained for two types of interface-engineered junctions with either YBCO or YbBCO as the counter-electrode material. The solid lines are drawn by eye as guides.

taper of 20° independent of the edge orientation in a wafer. After etching, the samples were heated to the temperature for the subsequent layer deposition and maintained at that temperature for 10 min. An activated oxygen flux from an ECR plasma source was supplied during the annealing process. The junction width was fixed at 4 μm throughout the present work.

Fig. 1 summarizes the substrate temperature dependence of I_c at 4.2 K averaged over 16 junctions in a chip, for the two different counter-electrode materials. In either case, the I_c values increase with increasing substrate temperature, but the substrate temperature at which a given I_c value is obtained differs by about 20–40 °C between the two types of junctions. This implies that the difference in the counter-electrode materials has some influence on the interface-barrier formation, though we could not observe any significant difference in the junction characteristics between YBCO and YbBCO junctions with a similar I_c value. Another interesting point to note in Fig. 1 is that, in both cases, the dependence of I_c on the substrate temperature becomes stronger in the low-temperature region. This may indicate the existence of some threshold in the thermodynamics in the interface-barrier formation. Unfortunately,

however, we do not fully understand the details yet.

3. Junction characteristics

Fig. 2 shows the $I_c R_n$ values as a function of J_c obtained for junctions on various wafers processed at various substrate temperatures. Similar data reported by two other research groups [3,10] are also plotted in the same figure for comparison. We can see that the experimental data from three independent research groups roughly coincides, implying that Fig. 1 depicts the general features of IEJs. An interesting feature seen in Fig. 1 is that the $I_c R_n$ values approximately scale with the square root of J_c in the J_c region below 10^4 A/cm^2, and then seem to saturate at around 3 mV at higher J_c. However, we noticed that the $I_c R_n$ values in the high-J_c region often exhibited similar square-root behavior as long as the junctions were on the same wafer, i.e., processed under the same conditions.

The scaling of $I_c R_n$ with the square root of J_c has been confirmed for grain boundary junctions as well as for PBCO barrier junctions, and is as-

cribed to the existence of different transport channels for Cooper pairs and quasiparticles; that is, Cooper pairs transfer by direct tunneling while quasiparticles can also flow by resonant tunneling [11–13]. The existence of similar scaling behavior seems to indicate that the current transport in IEJs can be understood within the same theoretical framework. We have confirmed that this is actually the case for IEJs in the low-J_c region, as described below.

Fig. 3 shows differential conductance versus voltage (dI/dV–V) characteristics observed for an IEJ with J_c of 3.4×10^3 A/cm^2 at various temperatures ranging from 4.2 to 60 K. The dI/dV profiles can be characterized by a slightly nonlinear increase in the conductance at high bias voltages, which is essentially independent of the temperature, and a temperature-dependent symmetrical dip with its minimum at zero voltage. We found that the nonlinear behavior at high voltages was fit quite well by $V^{4/3}$, as shown by the dotted line in the figure. This indicates that inelastic tunneling via two localized states in the barrier certainly plays a part in the quasiparticle current transport in the junction at high voltages [14]. We think this
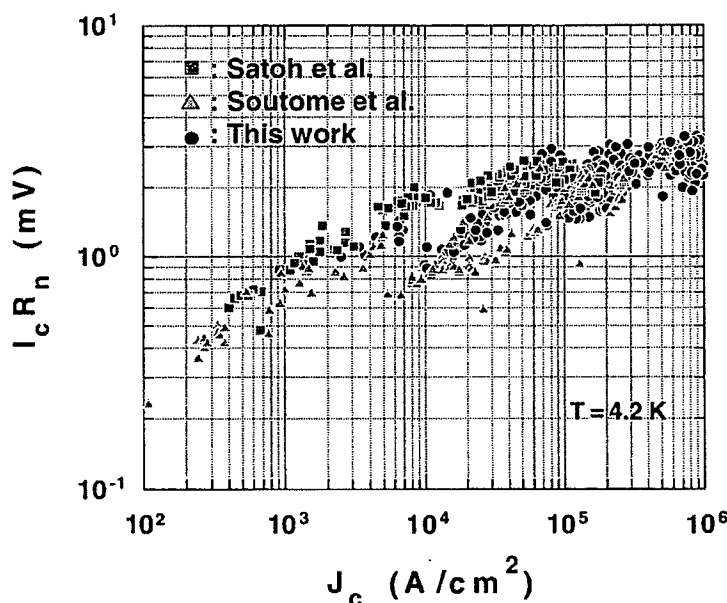
Fig. 2. $I_c R_n$ product values as a function of J_c obtained for interface-engineered junctions processed under various conditions.
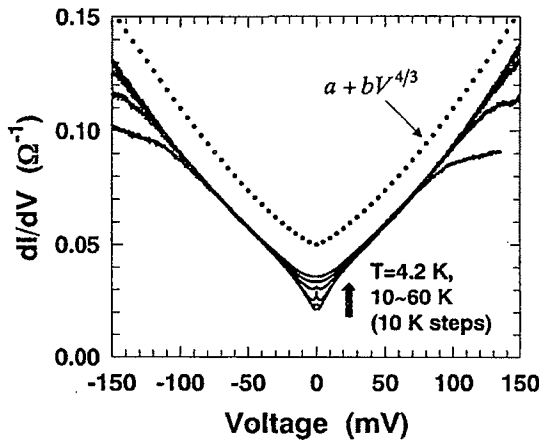
Fig. 3. Differential conductance versus voltage characteristics observed at various temperatures ranging from 4.2 to 60 K for an interface-engineered junction with $J_c = 3.4 \times 10^3$ A/cm².

offers strong evidence that IEJs with low J_c are tunnel junctions with an insulative barrier containing a high density of localized states in it. The symmetrical dip around zero voltage would be a remnant of a superconducting gap structure smeared out by a thin normal conducting or a reduced-T_c layer adjacent to the tunnel barrier.

The dI/dV profile of IEJs having J_c exceeding 10^4 A/cm² differs considerably from that of low-J_c junctions. Fig. 4 depicts the temperature depen-
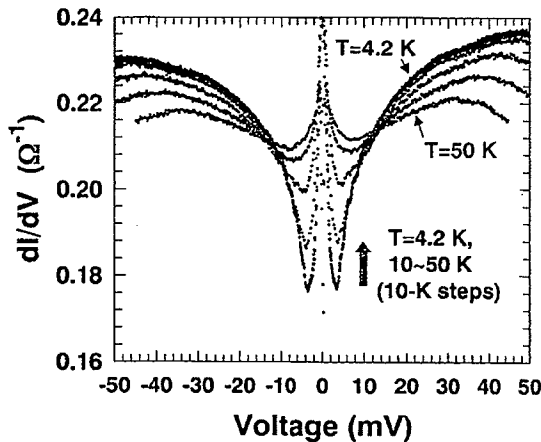
Fig. 4. Differential conductance versus voltage characteristics observed at various temperatures ranging from 4.2 to 50 K for an interface-engineered junction with $J_c = 5.5 \times 10^4$ A/cm².
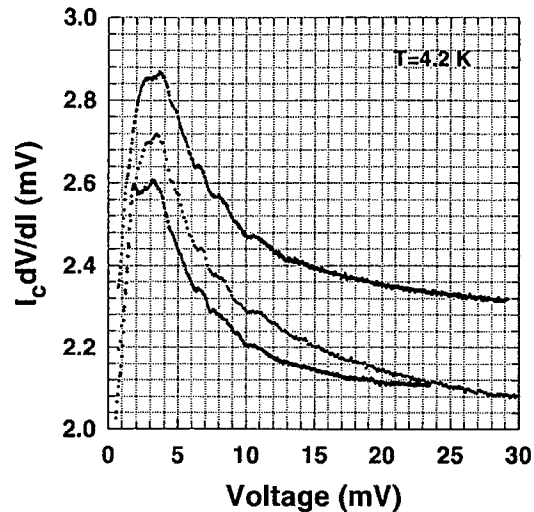
Fig. 5. dV/dI characteristics in the sub-gap region at 4.2 K for three different specimens.

dence of the dI/dV profile observed for a junction with J_c of 5.5×10^4 A/cm² at 4.2 K. The differential conductance does not exhibit a rapid increase at high voltages. Moreover, the differential conductance at high voltages increases gradually with decreasing temperature. Such behavior is certainly beyond the scope of a tunneling picture, and indicates the presence of a metallic channel within the junction. Another feature seen in Fig. 4 is the existence of fine structures in the superconducting gap region. The structure is reproducible, as shown in Fig. 5, as magnified differential resistance profiles for three different specimens.

We can find two plausible explanations in the literature for the fine structure in the sub-gap region. One is the Andreev levels formed in a clean superconductor–normal–superconductor (SNS) junction [15]. The Andreev levels are formed due to the interference of wave functions of quasiparticles in the N region which are Andreev reflected at the SN interfaces. Although the energy of the Andreev levels is usually dependent on the phase difference between the two superconducting banks, the presence of a point impurity having a large reflection coefficient in the SNS channel makes them almost phase insensitive [16]. Such levels could be observed as nearly equidistant

singularities in dI/dV profiles. The spacing between the Andreev levels is approximately given as $\Delta E \approx \pi \hbar v_F / d$, where v_F is the Fermi velocity in the N-layer and d is the length of the N-layer. A serious problem concerning the interpretation of the experimentally observed fine structure as the Andreev levels is its small spacing between singularities amounting to 3–5 mV. This requires an anomalously small v_F/d value, which does not seem to be valid when we take into account the short mean-free path in high-T_c superconductors.

A more plausible explanation would be the so-called "sub-harmonic gap structure (SGS)" originating from the process of multiple Andreev reflections in short SNS junctions [17]. The SGS appears as singularities at voltages $V_n = 2\Delta/en$, $n = 1, 2, 3, \ldots$, where Δ is the superconducting gap of the junction electrodes. The major structure below 10 mV seen in Fig. 5 may be assigned as the SGS with $n \geqslant 3$ for $2\Delta \approx 30$ meV. This interpretation, however, requires another explanation for the lack of the structure corresponding to $n = 1$ and 2. Moreover, the experimental profiles below 10 mV seem to include more complicated structures than that expected from this simple SGS model. One possible solution to this apparent discrepancy may be the introduction of a more complex SNcNS (here c denotes the constriction) model in which the proximity effect in the SN bilayers is taken into account. Aminov has shown that, in the case of an SNcNS structure, new resonances appear at $V_n = (\Delta_S - \Delta_N)/en$, $V_n = 2\Delta_N/en$, and $V_n = (\Delta_S + \Delta_N)/en$, due to the multiple Andreev reflections within the junction, where Δ_S and Δ_N are superconducting gaps in the S- and N-layer, respectively [18]. The relative importance of each process, and, thereby, the amplitude of resonance peaks in dI/dV profiles depends on the structure of individual junctions. Unfortunately, this makes it difficult to conclude specifically whether the fine structure seen in our dI/dV profiles can be assigned as the SGS in SNcNS junctions or not.

4. Unsolved problems

The universal scaling of $I_c R_n$ with the square root of J_c, and the nonlinear differential conduc-

tance which fits well with $V^{4/3}$ in IEJs with J_c less than 10^4 A/cm^2, forces us to think that the junctions in this regime can be classified as SIS or SNINS junctions with localized states in the barrier, and that Cooper pairs in the junctions transfer by direct tunneling while the quasiparticle current is dominated by resonant tunneling. This simple picture, however, does not seem to coincide with the quasilinear temperature dependence of I_c, as seen in Fig. 6 (two figures at the bottom). The nonexponential dependence of I_c on temperature,
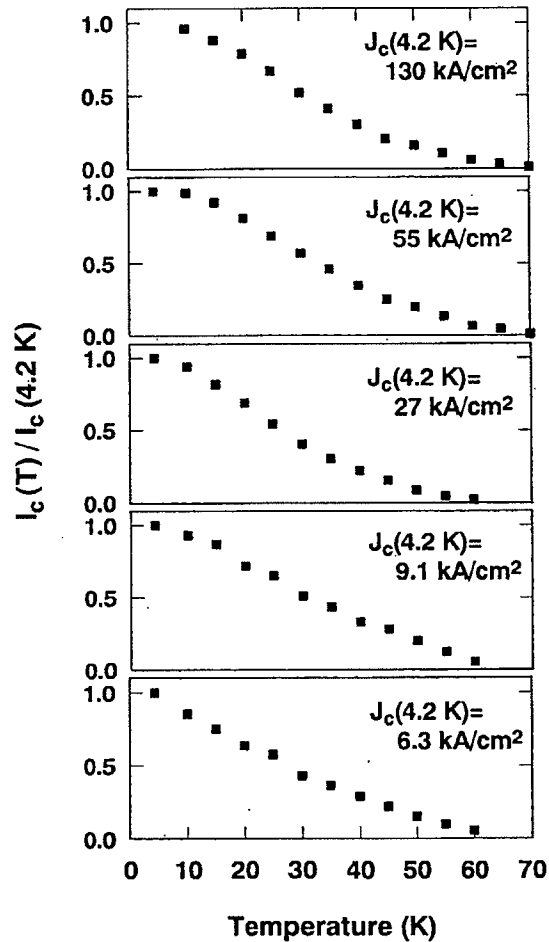
Fig. 6. Temperature dependences of I_c observed for interface-engineered junctions with various Josephson critical current densities at 4.2 K ranging 1.3×10^5–6.3×10^3 A/cm^2.

at high temperatures, and the lack of a saturation tendency in the low-temperature region are certainly beyond the scope of the SNINS model, and remind us of dirty point contacts [19]. However, if the Josephson current in these junctions is actually dominated by point contacts within an insulating barrier, we have to seek another rational explanation for the peculiar scaling relationship between I_cR_n and J_c.

The temperature dependence of I_c in IEJs in the high-J_c regime is more SNINS-like, as seen in the top three figures in Fig. 6. This does not conflict with the SNcNS model with a low transmission probability in the metallic channels. One curious aspect with high-J_c IEJs is that they often exhibit a scaling behavior in their I_cR_n versus J_c characteristics, similar to that observed for low-J_c junctions. Such scaling has been observed only among junctions fabricated simultaneously on the same wafer. In this sense, this scaling behavior is not universal, but, here again, we are required to consider a rational explanation other than that of the direct- and resonant-tunneling framework.

The mechanism of J_c variation in the high-J_c region due to process conditions is not clear at present. We can think of three possible reasons; variations in the N-layer thickness and in transmission probability of metallic channels, and the change in the number of the metallic channels within the junction area. A slight increase in the maximum I_cR_n values with J_c may be a consequence of the N-layer thickness variation, but this does not seem to dominate the J_c variation over the two orders of magnitude seen in Fig. 2. It is not easy to distinguish the other two mechanisms from each other. One possibility would be to observe the change in dI/dV profiles with an increase in the J_c values. Unfortunately, we have not succeeded in observing the dI/dV profile of high-J_c junctions in a wide voltage range because of the breakdown of superconductivity in the electrodes due to the large current flowing in the junction.

5. Summary

We investigated the current transport mechanism in interface-engineered junctions. We found

that the junction characteristics can be classified into two groups in accordance with their J_c values. The borderline between the low-J_c group and the high-J_c group lies at around $J_c = 1 \times 10^4$ A/cm^2. In the low-J_c region, I_cR_n values scaled universally with the square root of J_c, and the contribution of elastic and inelastic tunneling processes, at least to the quasiparticle currents, was confirmed through the measurement of dI/dV profiles. However, some questions still remain concerning the transport of Cooper pairs in this region.

In the high-J_c region, an SNcNS model with low transmission probability of metallic channels seems to be most appropriate to account for the overall features of experimentally observed junction characteristics. Further investigations, however, are definitely required to identify the origins of the fine structure appearing in the dI/dV profiles as well as of the variation in J_c values over two orders of magnitude, due to process conditions.

Acknowledgements

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Characteristics of interface-engineered Josephson junctions using a YbBa$_2$Cu$_3$O$_y$ counterelectrode layer

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We have fabricated interface-engineered junctions with YbBa$_2$Cu$_3$O$_y$ as the counterelectrode. The junctions fabricated on YBa$_2$Cu$_3$O$_y$ base electrodes exhibited excellent Josephson characteristics with the 1σ-spread in I_c as low as 5.4% for 16 junctions with an average I_c of around 1 mA. We also confirmed that the 1σ in I_c correlates with the surface morphology of the base-electrode layer, indicating that further improvements in 1σ would be possible by advancing the thin-film growth technology. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1428115]

The interface-engineering technique proposed by Moeckly and Char[1] is regarded as the most promising method for fabricating high-temperature superconductor Josephson junctions for digital circuit applications, because of the resultant high uniformity in junction characteristics.[2,3] The basic concept of the interface engineering is to create a thin barrier layer by damaging the base-electrode surface using ion bombardment and then recrystallizing it during the subsequent counterelectrode deposition process. Even a conventional ion-milling process to form a ramp-edge structure in the base-electrode layer was confirmed to be sufficient to form an interface barrier.[2]

The electrical properties of interface-engineered junctions (IEJs) are known to be extremely sensitive to the substrate temperature and the oxygen atmosphere during the annealing process prior to the counterelectrode deposition. In the previous paper,[4] we demonstrated that annealing in an electron-cyclotron-resonance (ECR) activated oxygen flux and subsequent deposition of YBa$_2$Cu$_3$O$_7$ (YBCO) counterelectrodes by sputtering were advantageous in that they resulted in weaker substrate-temperature dependence of junction critical current (I_c) than was possible by other methods. Unfortunately, however, the I_c value appropriate for the fabrication of single flux quantum (SFQ) circuits could be obtained only at a relatively low substrate temperature range, which conflicted with the complete c-axis oriented growth of the counterelectrode layer.

The operation of a SFQ circuit is based on the transmission and storage of a single flux quantum by superconducting loops, which are connected in series or in parallel.[5] This operation principle results in the inductance L of the superconducting loops in SFQ circuits being restricted according to the inequality $0.5\Phi_0 < LI_c < 1.5\Phi_0$, where Φ_0 denotes the flux quantum ($h/2e$), and this limits the maximum I_c of Josephson junctions in practical circuits. For the reliable operation of a SFQ circuit at high temperatures, I_c must be sufficiently large compared with the thermal fluctuation current $I_T = (2\pi/\Phi_0)k_B T$. The inclusion of even a small amount of a-axis oriented grains in the counterelectrode YBCO film results in a significant increase in L, which

makes it impossible to operate a SFQ circuit correctly at a desired temperature.

The trade-off problem between I_c and L we encountered for the sputter-deposited YBCO counterelectrode layer could be solved if we adopted YbBa$_2$Cu$_3$O$_7$ (YbBCO) as the counterelectrode, because it can grow with complete c-axis orientation in a far wider temperature range than is possible with YBCO.[6-8] This letter reports our successful fabrication of IEJs with YbBCO as the counterelectrode.

The YbBCO and YBCO films used in the present work were grown on SrTiO$_3$(100) (STO) substrates using an off-axis sputtering system. Both films were deposited in a 200 mTorr mixture of 70% Ar and 30% O$_2$. Figure 1 shows the volume fractions of a-axis oriented grains in the films as functions of the substrate temperature. The volume fractions were estimated from the x-ray (200) diffraction intensity relative to (004). It is apparent that the curve for YbBCO shifts to the lower temperature side by approximately 100 °C compared with that for YBCO, indicating that by adopting YbBCO as the counterelectrode the substrate temperature can be reduced significantly while maintaining the quality of the wiring layer.

Ramp-edge structures were produced on the bilayer composed of the STO insulation layer and 200-nm-thick YBCO base-electrode layer by the two-step etching technique for a clean surface.[9] The STO layer was patterned using a reflowed resist mask together with Ar ion milling,
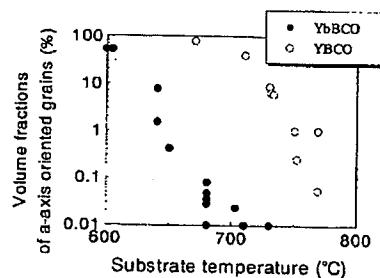
FIG. 1. The volume fractions of a-axis oriented grains in the films as functions of the substrate temperature for the counterelectrode deposition. The dot plots are results of junctions using YbBCO counterelectrodes and the circle plots are results of all-YBCO junctions.

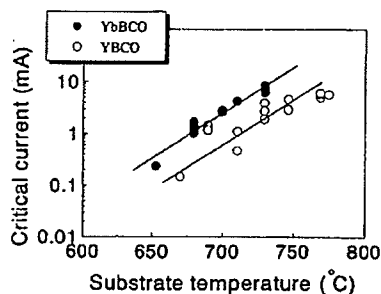[a]Electronic mail: hiroshi.katsuno@toshiba.co.jp

FIG. 2. The junction critical currents averaged over 16 junctions as functions of the substrate temperature for the counterelectrode deposition. The counterelectrodes of these junctions were fabricated by YbBCO (dots) and YbBCO (circles), respectively.

while rotating the substrate. The Ar-ion beam was applied to the substrate surface vertically. After removing the resist, the remaining STO layer and the YBCO base-electrode layer were etched with 30° tilting. The resultant ramp-edge angles were formed at about 20°.

The samples were heated to the deposition temperature which ranged from 650 to 730 °C for the fabrication of the counterelectrode layer in the sputtering chamber, and annealed for 10 min in an activated oxygen flux from an ECR plasma source at 2.1 mTorr. The ramp-edge surface of the YBCO base electrode became the barrier as samples were annealed. Successively, a 300-nm-thick YbBCO counterelectrode layer was deposited *in situ*. The YbBCO layer was patterned as the counterelectrode after covering the wafer surface with a 1-μm-thick Au film for contact pads. The junction width was fixed at 4 μm throughout this study. Then, the samples were annealed at 400 °C in O_2 for 24 h. The critical temperatures (T_c) of each electrode were exceeding 80 K.

Figure 2 compares the substrate temperature (T_{sub}) dependence of I_c observed for junctions using a YbBCO counterelectrode with that for all-YBCO junctions. Each circle in Fig. 2 represents the I_c value at 4.2 K averaged over 16 junctions on a chip. Both types of junctions exhibited nearly exponential dependence of I_c on the substrate temperature, with a similar increasing ratio of approximately 3%/° C. An interesting point to note is that the I_c vs T_{sub} curve for YbBCO junctions seems to shift to the lower temperature side by approximately 30 °C compared with that for YBCO junctions. This implies that the characteristics of IEJs are influenced not only by the process conditions but also by the counterelectrode material itself. Unfortunately, we do not understand the details of this phenomenon.

The maximum I_c value of Josephson junctions usable in high-T_c SFQ circuits is estimated to be 0.4–0.5 mA at 30–40 K because of the restriction arising from inductance design.[10] Since the I_c value of IEJs at 4.2 K is approximately twice that at 30–40 K, the I_c value around 1 mA at 4.2 K is particularly important for SFQ circuit applications. Figure 2 indicates that such a junction can be obtained at T_{sub} of around 680 and 710 °C for YbBCO and YBCO junctions, respectively. The former temperature is high enough to obtain YbBCO films with negligible inclusion of a-axis oriented grains, as seen in Fig. 1, while the latter is far too low to obtain YBCO films with similar quality.
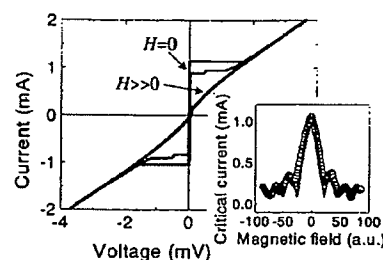
FIG. 3. The $I-V$ characteristics at 4.2 K using the YbBCO counterelectrode fabricated at 680 K. The inset shows the magnetic field modulation of I_c. The solid line in the inset is a fit to the Fraunhofer pattern.

Figure 3 shows the $I-V$ characteristics at 4.2 K and the Fraunhofer pattern observed for a YbBCO junction fabricated at 680 °C showing complete c-axis orientation in the counterelectrode. The junction exhibited excellent Josephson characteristics with the magnetic field modulation of I_c exceeding 90% and the $I_c R_n$ product of the junctions exceeding 2 mV. The curve included a weak hysteretic behavior with a small bump structure probably due to the parasitic LC resonance peculiar to a ramp-edge structure.[3] These characteristics were not different from those of YBCO junctions. It was confirmed that the weak hysteresis seen in the $I-V$ curve diminished at 30–40 K.

The $I_c R_n$ product gradually increased with an increase in I_c and ranged from 1 to 3 mV at 4.2 K in I_c ranging from 0.1 to 10 mA as seen in Fig. 4. The whole feature of Fig. 4 showed the $I_c R_n$ products had slightly weak dependence on I_c and scaled approximately with I_c^P where P ranged from 0.2 to 0.3.[2,11] The normal-state resistance R_n was also essentially independent of the temperature. These behaviors are different from Co-doped PBCO barrier junctions which are based on the localized states in the barrier,[10] which may imply the lesser barrier thickness or the smaller density of the localized states.

The temperature dependence of I_c was considerably different from that of superconductor–insulator–super conductor junctions. The critical current was proportional to $(1 - T/T_c)^2$ in the vicinity of T_c. With decreasing temperature, the I_c value showed the saturation behavior. Such behavior is a typical tendency of superconductor–normal metal–insulator–normal metal–superconductor junctions.[12]

The uniformity and reproducibility of the junction characteristics were investigated for 16 junctions, as seen in Fig.
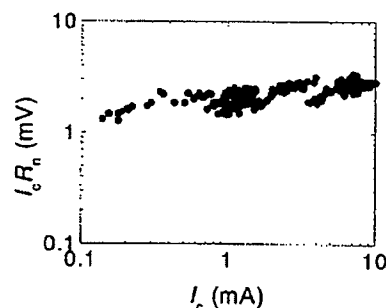

FIG. 4. The relation between I_c and the $I_c R_n$ product for junctions with YbBCO counterelectrodes at 4.2 K.
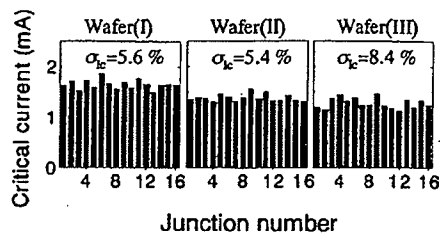
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FIG. 5. These graphs show the uniformity in three wafers at 4.2 K indepen-dently fabricated under the same process condition ($T_{sub} = 680\,°C$). The $\langle I_c \rangle$ values of each chip averaged over 16 junctions are estimated as 1.65, 1.39, and 1.28 mA, respectively.

FIG. 6. The relation between the 1 σ-spread in I_c and the relative area of precipitate observed on the surface of the isolation layer.

5. These chips were independently fabricated under the same process condition and were located at the same place in each wafer. We confirmed good reproducibility in I_c between wa-fers. The best uniformity obtained so far was a 1 σ-spread in I_c of 5.4%. This value was reproducible as long as the junc-tions were fabricated on a YBCO base-electrode layer of high quality. We found that the 1 σ-spread correlated strongly with the surface morphology of the isolation/base-electrode bilayers. Figure 6 shows the relation between the 1 σ-spread in I_c and the relative area of precipitate observed on the surface of the isolation layer by a scanning electron micro-scope prior to the fabrication of a ramp-edge structure. Ac-cording to the deposition condition, there were small precipi-tates (0.1–1 μm in diameter), which could not be detected by x-ray diffraction, on the bilayer. As a result of Auger electron spectroscopy, these precipitates are thought to originate mainly from the slight deviation of the atomic composition from stoichiometry in the YBCO base-electrode layer located underneath the isolation layer. It was shown that the 1 σ-spread in I_c is affected strongly by the quality of the base-electrode layer. In other words, there is an opportunity to reduce the 1 σ-spread further by improving the quality of the base-electrode layer.

In summary, we have fabricated interface-engineered junctions suitable for the construction of SFQ circuits based on high-temperature superconductors by adopting YbBCO as the counterelectrode. The junctions exhibited excellent Jo-

sephson characteristics together with the 1 σ-spread in I_c as low as 5.4%. Further reduction in 1 σ would be possible by improving the quality of the base-electrode layer.
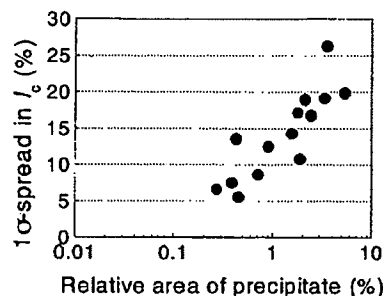
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Interface-modified YBCO ramp-edge Josephson junctions by deionized water

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Abstract

We have investigated $YBa_2Cu_3O_{7-x}$ (YBCO) ramp-edge Josephson junctions by reacting the ramp-edge interface with deionized water. $YBa_2Cu_3O_{7-x}/PrBa_2Cu_3O_x$ (YBCO/PBCO) films were deposited on $SrTiO_3(1\,0\,0)$ by on-axis KrF laser deposition. After patterning the bottom YBCO/PBCO layer, the ramp edge was cleaned by Br-in-ethanol and then reacted with deionized water. The top YBCO/PBCO layer was deposited and patterned by photolithography and ion milling. We measured the current–voltage (I–V) characteristics, magnetic field modulation of the critical current and microwave response at 10 GHz. The 20-minute water-immersed junction showed resistively shunted junction (RSJ)-type I–V characteristics, while others exhibited flux-flow behaviour. The average values of I_c, R_n and I_cR_n of these RSJ-type junctions were 4 mA, 0.1 Ω and 400 μV, respectively, and Shapiro steps were fitted well by the microwave characteristic parameter $\Omega\,(= hf/2eI_cR_n) = 0.18$.

1. Introduction

For the manufacture of electronic devices based on high-temperature superconductors (HTSC) there have been a great number of efforts to establish a reliable Josephson junction (JJ) fabrication process. Due to the extremely short coherence length of HTSC the control of the interface on this length scale is crucial. Since the coherence length in the ab-plane is longer than that in the direction of the c-axis in $YBa_2Cu_3O_{7-x}$ (YBCO), the JJ of this material has usually been made in the ab-direction using the ramp-edge geometry. Attempts to create artificial-layered tunnel barriers have not been very successful.

Several years ago Moeckly and Char fabricated interface-modified ramp-edge type HTSC JJ without depositing any artificial barrier [1]. The main idea is that the YBCO surface can be modified into a non-superconducting material after being exposed to appropriate ion damage. Since this study, there has been a great deal of research on interface-modified ramp-edge-type HTSC JJ using various methods for interface modification, such as plasma treatment [1–3], ion beam damage [4–7], chemical treatment [7] and base electrode doping [9]. Wen *et al* argued that the barrier layer, composed of Ba-based cubic perovskite phase, is certainly a derivative compound of YBCO [10]. On the other hand, Huang *et al* reported that the barrier layer of plasma-treated

junctions consists of a cation-disordered non-superconducting cubic structure [11].

In addition, the reproducibility of ramp-edge-type HTSC JJ is still under debate, hence Schoop *et al* have carried out a detailed study of ramp formation by ion beam techniques [12]. Moeckly recently succeeded in producing a c-axis trilayer interface-engineered JJ [13]. However, the reproducibility is still in question.

It has been shown that YBCO decomposes in water to CuO, $Ba(OH)_2$, Y_2BaCuO_5 and evolving oxygen [14, 15]. Therefore, in this study we have tried to make JJ using the barrier formed by this chemical reaction instead of by physical damage.

2. Fabrication

Josephson junctions were fabricated using thin films deposited by pulsed laser ablation. The optimized parameters for pulsed laser deposition of YBCO thin films were as follows: oxygen partial pressure = 750 mT, substrate temperature = 800 °C and laser energy density = 1.4 J cm^{-2}. The zero-resistance critical temperature was ~90 K with transition width smaller than 1 K [16]. The deposition parameters for $PrBa_2Cu_3O_x$ (PBCO) thin film were the same as those for YBCO. YBCO (220 nm)/ PBCO (100 nm) bilayers are deposited onto single-crystal
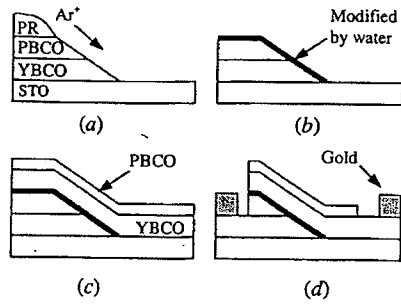
Figure 1. Schematic diagrams of the overall junction fabrication process: (a) formation of the ramp edge, (b) ramp-edge modification by water, (c) deposition of counter-electrode and (d) lift-off of gold contact pads.

SrTiO$_3$(100) substrates. After conventional photolithography for the base electrode, Ar-ion milling was performed using a Kaufmann-type ion source at an incident angle of 65° to obtain ramp edges with small angles. The energy of the ion beam was 400 eV and the current density was 1.0 mA cm^{-2}. After edge formation, the dead surface layer was removed by a subsequent 0.2% in volume Br-in-ethanol cleaning for 20 s [17]. We then immersed it in deionized water at room temperature (RT) after rinsing it with methanol and acetone several times. The resistivity of the deionized water was 16 MΩcm. Base electrodes with modified edges were immediately attached onto a heater block and transferred to a deposition chamber. The counter-electrode YBCO (220 nm)/ PBCO (40 nm) thin films were deposited using the same parameters as for the base electrode. The samples were patterned into structures of ramp-edge-type junctions by using
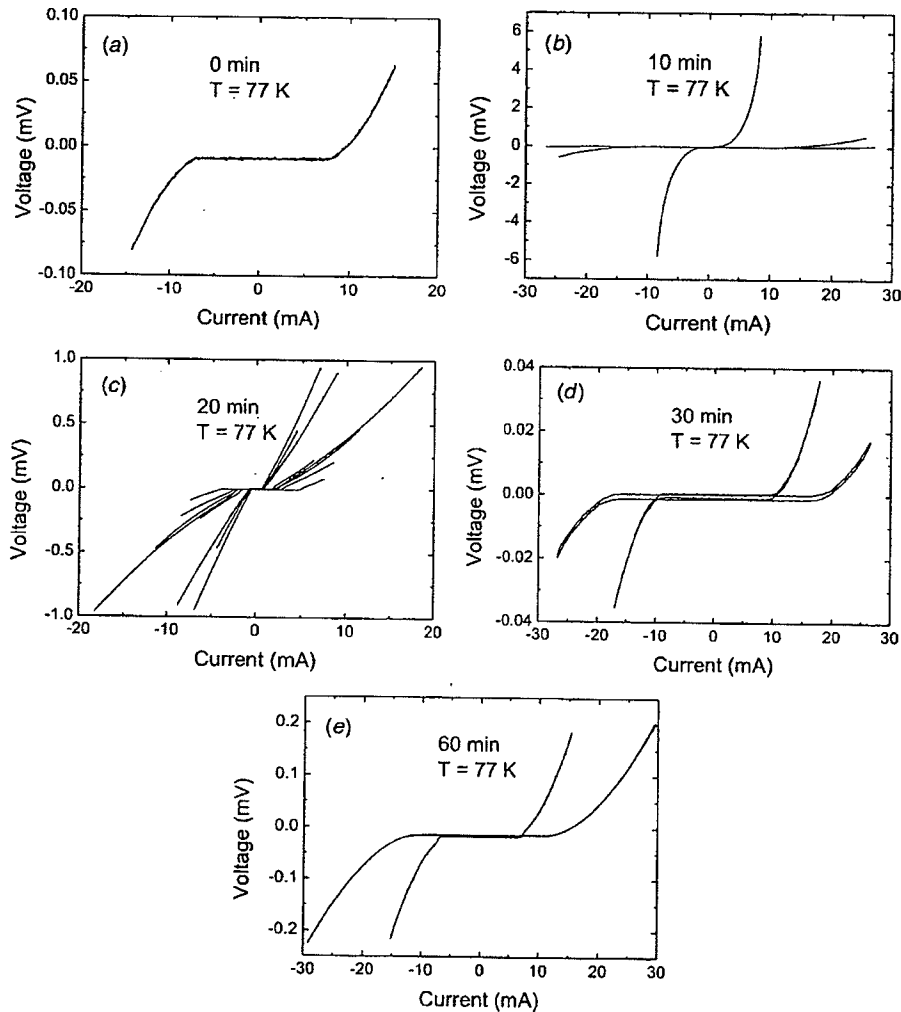
Figure 2. Current–voltage characteristics of junctions at 77 K for different water immersion times: (a) 0 minute, (b) 10 minutes, (c) 20 minutes, (d) 30 minutes and (e) 60 minutes.
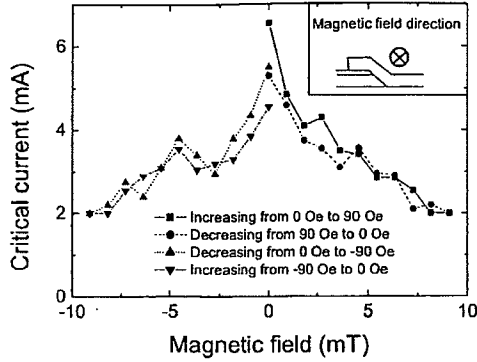
Figure 3. Magnetic field modulation of the critical current of an RSJ-type junction at 77 K.
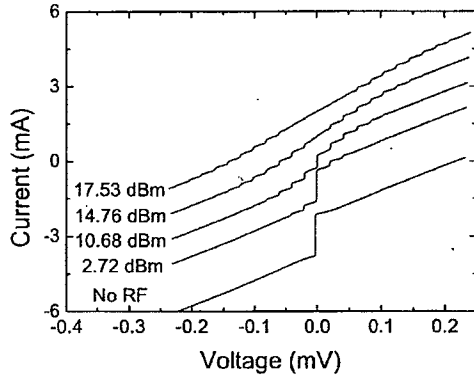
Figure 4. Current–voltage curves for the same junction in figure 3 exposed to a 10-GHz signal at various power levels.

Figure 5. Dependence of the normalized Shapiro-step heights on the microwave current for $n = 0, 1, 2$ and 3 of the same previous junction. The lines show the RSJ simulation results with $\Omega = 0.18$.

photolithography and Ar-ion milling. Finally, gold contact pads were formed by the conventional lift-off process. The process sequence is shown schematically in figure 1. Typically, we have annealed our junctions at 450 °C for 30 min with oxygen flow 50 sccm in the chamber.

Each chip of 10 mm × 10 mm size contains nine sectors, each of which is composed of 22 junctions with a junction width of 4 μm. To check the transport properties of each electrode, four-probe test patterns of micro-bridge type were also included in both the bottom and the top layers. We measured the current–voltage (I–V) characteristics, magnetic field dependence of the critical current and Shapiro steps by dipping samples in liquid nitrogen.

3. Results

The immersion time in the deionized water was varied as 0, 10, 20, 30, 40 and 60 min. Figures 2(*a*)–(*e*) show the *I*–*V* characteristics for each chip. The 20-minute junctions showed RSJ-like *I*–*V* characteristics at 77 K as in figure 2(*c*), which still have excess currents. The average values of I_c, R_n, and I_cR_n of 10 junctions are 4 mA, 0.1 Ω and 400 μV, respectively. Most of the other junctions, with either shorter or longer immersion

time, showed flux-flow-type with J_c between 1×10^6 and 2×10^6 A cm^{-2}, which implies that there exists little barrier between two YBCO electrodes. The resistance grows from 0.01 Ω for the 0-minute junction to 0.1 Ω for the 20-minute junction and suddenly returns to 0.01 Ω again for the 30-minute junction. Then the resistance grows slowly again as the immersion time increases. The critical current behaves in the opposite way. We will discuss this behaviour in more detail later.

The magnetic field dependence of the critical current of a typical RSJ-type junction is plotted in figure 3, where the first minimum is found at about 3 mT. As Heinsohn *et al* pointed out [18], junctions with an excess current do not show a clear Fraunhofer-like pattern. Assuming that the junction width (which, in this case, is the thickness t of the bottom film as indicated in the inset of figure 3) is shorter than the Josephson penetration depth $\lambda_J = [h/4\pi\mu_0 eJ_c(d + 2\lambda_L)]^{1/2}$ we can roughly estimate the penetration depth $\lambda_L \approx \Phi_0/(2tH_{min}) \approx$ 1.6 μm, which is somewhat larger than the literature value of YBCO at 77 K, i.e. $\lambda_{ab} \approx 0.16$ μm, or $\lambda_c \approx 1.1$ μm [19].

Figure 4 shows the microwave (10 GHz) responses of the same JJ of figure 3. We can observe current steps at $V = nV_0$ where $V_0 = hf/2e = 20.7$ μV. The Shapiro step amplitude is plotted as a function of microwave current in figure 5. The theoretical value was found from the RSJ current source

model [20]. The fitting parameter $\Omega = hf/2eI_cR_n$ varies from 0.10 to 0.90. As Ω grows, the first maxima for $n > 0$ increases so that it is easy to find the optimal fitting value of Ω by matching the first maximum. The most probable value of Ω was 0.18, which is inconsistent with the calculated value from the I–V characteristics in figure 4 where $\Omega = hf/2eI_cR_n = V_0/I_cR_n = 20.7\ \mu V/61.5\ \mu V = 0.34$. This results from the excess current, which has not been considered in the RSJ model. Heinsohn *et al* have also observed this kind of inconsistency in their interface-engineered JJ; when the temperature was lowered the excess current became significant [18].

4. Discussions and summary

What happened to the YBCO surface on immersion in water? After decomposition of the YBCO surface by water, the reaction product $Ba(OH)_2$ dissolves easily. The other products, i.e. CuO and Y_2BaCuO_5 remain as a barrier for JJ. However, when the etching time in deionized water is too long, we speculate that the original YBCO phase was exposed to the surface again as the barrier materials were washed away. This results in high critical currents of the flux-flow-type junctions etched in deionized water for more than 30 minutes.

In summary, we have made ramp-edge JJs using the barrier obtained from YBCO and water reaction. The optimum time for immersing in water is about 20 minutes, and this JJ showed RSJ-like behaviour with an excess current. We have measured the I–V characteristics, magnetic field modulation of the critical current and microwave response. However, there are still many problems which must be overcome before reproducible and controllable JJs can be achieved by this method.

Acknowledgments

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RAPID COMMUNICATION

'Interface-engineered' high-T_c Josephson junctions: a possible mechanism of operation

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Abstract. The mechanism of operation of the 'interface-engineered' high-T_c Josephson junctions with ion-modified barrier has been discussed. The analysis is performed for a YBaCuO base electrode modified by Ar^+ and O^+ ions. Using the diffusion coefficients of each YBaCuO component it is shown that at the counter-electrode deposition temperature (about 780 °C) the O and Cu defects anneal out and the Ba and Y sublattice disorder remains the only factor to play an important role in YBaCuO interface modification. The nature of the barrier in these devices seems to be very complicated, probably 'insulator/normal conductor/superconductor with reduced critical temperature' and the junctions can be described as S–I–N–S′–S.

Ramp-type Josephson junctions fabricated without any deposited interlayer and in which the barrier is created by an interface modification have attracted great attention recently [1–4]. In this method of fabrication a YBaCuO ramp (the base electrode) is treated with Ar^+ or O^+ ions and subsequently annealed prior to the deposition of the top electrode. These devices appear to be reproducible and with I–V characteristics well described by the resistive shunted junction (RSJ) model. The modulation of the critical current with an external magnetic field indicates the formation of a homogeneous barrier layer at the interface. The temperature dependences of the critical current and of the normal resistance suggest the existence of a non-superconducting barrier. However, the nature of the barrier is still under debate and the mechanism of operation of these junctions is unclear.

Recently [5] we have made an attempt to shed light on the nature of the interface-engineered junctions. We supposed that these devices can be described as S–N–S devices, where the normal region is created by ion modification similarly to our e-beam-modified or oxygen-ion-modified weak links [6–10]. The thickness of the modified region in the layer was calculated for a typical experimental ion energy of 500 eV and it was found to be only 2–3 nm. Obviously the plasma treatment creates a barrier region only a few YBaCuO unit cells thick. This extremely thin layer actually determines the length of the created weak link and is responsible for the excellent properties of these junctions. Such a barrier thickness is consistent with the recent observation [11] by

transmission electron microscopy of a 2–3 nm thin region at the YBCO interface with a different structure.

However, there is still a problem that has to be solved precisely. During the deposition of the top YBaCuO layer a thermal annealing occurs at a temperature of about 780 °C. We suggested [5] that the displacement of oxygen ions alone is important for the depressing of T_c and during the high-temperature treatment a significant part, but not all of the induced oxygen defects will be annealed out. A rough estimation using the value of the activation energy for oxygen diffusion was made [5] leading to a reasonable agreement with the experimental data. However, recently some strong indications have been given that not the oxygen sublattice disorder, but rather the cation disorder is probably the primary cause of the Josephson effect in these devices [11]. The authors stated that these junctions are stable under high temperature oxygen anneals for several hours, which means that the oxygen diffusion at 780 °C probably cannot play the major role in these devices. In this communication we try to present a more accurate analysis of this still open question, taking into account also the created cation defects.

The well known Monte Carlo code TRIM [12] can be used for this purpose, similarly to our previous work [5, 13]. The profiles of the total ion energy loss together with the energy absorbed by each YBaCuO component are plotted in figure 1 in the case of 500 eV argon ion modification. The YBaCuO critical temperature reduction is related to the total energy losses of the ions and thus to the average number of defects produced, as already shown

Table 1. Averaged critical temperatures calculated for 100 nm YBaCuO film irradiated with 200 keV O^+ compared to the experimental data [15].

Dose (ions cm^{-2})	T_c (K) calculated using energy losses of all YBaCuO elements	T_c (K) calculated using energy losses of only Y, Ba and Cu	T_c (K) experimental [15] (middle of transition)
1×10^{13}	81	84.5	81
2×10^{13}	75	81.5	80
4×10^{13}	62.5	75	74
6×10^{13}	50	68.5	67
8×10^{13}	38	62.5	62.5
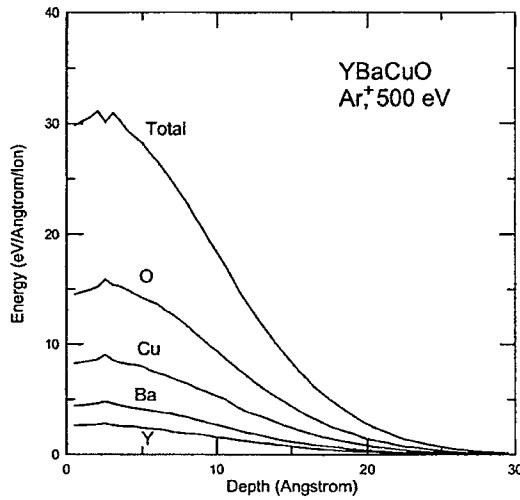
Figure 1. Calculated total energy losses and energy losses for each component in YBaCuO film for modification by argon ions with energy of 500 eV.

Table 2. Parameters of the Gaussian fits of the curves from figure 1.

	Total	Y	Ba	Cu	O
y_0	0.295	0.018	0.096	0.063	0.263
x_c	1.70	1.21	1.55	1.79	2.25
2σ	16.30	16.85	16.35	16.48	15.72
A	618.9	56.6	93.4	175.3	294.7

Table 3. Diffusion coefficients of the YBaCuO components.

	D (cm^2 s^{-1}) at 780 °C	Reference
O	10^{-8}–10^{-10}	[16-18]
Cu	10^{-13}	[19]
Ba	10^{-20}	[20]
Y	10^{-33}	[20]

by Summers *et al* [14]. As seen in figure 1 about one half of created defects are oxygen defects. They probably annealed out almost completely [15] as early as 500 °C. However, after such a treatment the critical temperature does not recover to its original value [15]. This fact shows that not only oxygen defects, but also the cation sublattice disorder has an important effect on the T_c degradation.

We calculated critical temperatures similarly to our earlier work [13] for a 100 nm YBaCuO film irradiated with 200 keV oxygen ions. For this energy the projected range of the ions is larger then the film thickness and therefore only the effects of produced defects are significant. Additionally, the critical temperature depth profile is nearly uniform and one can make straightforward comparison of calculated and measured critical temperatures. The results of these calculations are presented in table 1. In the second column data are given for calculation using the total energy losses of the ions and in third column assuming that oxygen defects are completely annealed out. The calculated critical temperatures, presented in table 1, were averaged over the film thickness.

The measured T_c after a 500 °C thermal treatment [15] (last column in table 1) is in good agreement with the value

calculated using only Y, Ba and Cu defects. Obviously the cation disorder causes about one half of the critical temperature reduction and remains the main reason for the T_c reduction even after a 500 °C anneal. These results encourage us to consider also the case of interface-engineered junctions.

All curves shown in figure 1 can be fitted quite well with a Gaussian function

$$F(x) = y_0 + \frac{A}{\sqrt{2\pi}\sigma} \exp\left[\frac{-(x - x_0)^2}{2\sigma^2}\right]. \quad (1)$$

Here y_0 is the baseline offset, A is the total area under the curve, x_c is the centre of the peak and σ is the standard deviation. Table 2 shows the parameters of the curves from figure 1.

During the thermal treatment of the base electrode and during the deposition of the counter-electrode a thermal diffusion occurs. For a Gaussian distribution the analytical solution of the diffusion equation is:

$$F_a(x) = \frac{A}{\sqrt{1 + 2Dt/\sigma^2}} \exp\left[\frac{-(x - x_0)^2}{2\sigma^2 + 4Dt}\right] \quad (2)$$

where D is the diffusion coefficient and t is the annealing time. Obviously an annealing takes place when $Dt \geqslant \sigma^2$. For ions with energy of 500 eV the standard deviation σ for all curves from figure 1 is about 0.8 nm for argon ions and about 1.1 nm for similar curves calculated for oxygen ions. Using $t \sim 10^3$ s as a typical time for the counter-electrode deposition, one obtains that the diffusion coefficient has to be greater then 10^{-17} cm^2 s^{-1} in order for created defects to anneal out completely.

Table 3 summarizes the diffusion coefficients found in the literature for oxygen [16–18] and copper [19] at temperature $T \cong 780\,°C$. The data for Ba and Y are available in the literature [20] for a different temperature interval and were extrapolated for 780 °C using the Arrhenius relation.

Obviously at 780 °C for oxygen and copper $Dt \gg \sigma^2$ and the ion-induced defects will be almost completely annealed out. Since the heat treatment at this temperature and for the same deposition time is not sufficient to cause changes in the disordered Ba and Y sublattices, their amount is likely to be the factor controlling for YBaCuO interface modification. On the basis of this result, we can conclude that the remaining Ba and Y sublattice displacements, which cannot be removed during the counterelectrode deposition at 780 °C, are responsible for the suppression of T_c and thus for the Josephson effect observed in these junctions. They can be misinterpreted in TEM investigations as a new (cubic) phase [2, 11] of YBaCuO or as an a-axis-oriented YBaCuO [21]. Probably similar is the mechanism of operation of the sandwich junctions YBCO/PBCO/YBCO [22] made by planarization of the base electrode by an Ar ion beam at 700 eV.

The remaining defects after such a thermal treatment are about 25% of the total defect amount (see figure 1). Because the critical temperature reduction is proportional to the average number of defects, this means that for the parameters of the fabrication process [1] an apparent ion dose will be about 2.4×10^{18} ions cm^{-2} at its maximum. For such a high dose this part of the barrier should be in an insulator state. The number of created defects drops rapidly inside the film and reaches a level equivalent the dose $\sim 6 \times 10^{13}$ ions cm^{-2}, which is needed to reduce the critical temperature to zero without annealing, at a depth of about 4 nm. This depth will be actually an effective barrier length of the junction. Deeper in the film a gradual transition from an insulator through a normal conductor to a superconductor with reduced critical temperature occurs. Hence, the nature of the barrier in these devices is likely to be very complicated, probably 'insulator–normal conductor–superconductor with reduced critical temperature' and the Josephson junctions can be described as S–I–N–S'–S. By choosing the appropriate ion energy and annealing conditions, it is possible to fabricate high-T_c Josephson junctions with a wide range of barriers ranging from almost S–N–S junctions to cases where the S–I–S mechanism is dominant.

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Structural variation of the interface-engineered layers in YBa$_2$Cu$_3$O$_{7-\delta}$ thin films

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Abstract

The atomic structures of interface-engineered YBa$_2$Cu$_3$O$_{7-\delta}$ (YBCO)/plasma-treated YBCO/a-axis YBCO 'trilayer' samples have been observed by transmission electron microscopy. The microstructures are compared by changing the plasma treatment conditions. The detailed structure of the interface or the barrier layer varies both from sample to sample and from place to place in the same sample. It is found that the interface structure depends on both the accelerating voltage and the atmosphere for the plasma treatment. The interfaces under high accelerating voltages (700 and 500 V) are strained, while strain-free barriers with different crystal structures are formed by the treatment under lower accelerating voltages (350 and 200 V). In the sample prepared in the mixed atmosphere of argon and oxygen, a kind of cubic structure is found at the interface, while in the sample fabricated in pure argon, besides the cubic structure, BaCuO$_2$ and Y$_2$O$_3$ are also observed in the interface. © 2001 Elsevier Science B.V. All rights reserved.

1. Introduction

Fabrication of superconductor–normal–superconductor (SNS) or superconductor–insulator–superconductor (SIS) Josephson junctions has been an attractive topic since the discovery of high T_c superconductors [1–4]. No matter the junctions are in the form of trilayers or edge designs using various normal materials as barriers, to make a thin (typically less than 10 nm), uniform barrier is the most difficult step in the fabrication.

Recently, Moeckly et al. have developed an interface-engineered junction (IEJ), in which no barrier deposition is involved [5,6]. IEJ barriers are fabricated from an amorphous layer that is made by an ion bombardment process. Radio frequency (RF) plasma discharge, Ar ion milling or electron cyclotron resonance (ECR) ion etching is usually used to make an amorphous layer, which is changed to a barrier layer through appropriate annealing and upper YBa$_2$Cu$_3$O$_{7-\delta}$ (YBCO) deposition processes [7], however, ion bombardment and recrystallization processes are quite complex. In particular, the latter process is closely related with disordered arrangement of cations, which depends on the former process. Thus, it is worthwhile clarifying the factors governing the

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recrystallization process. Huang et al. concluded that the interface barrier is cubic or pseudocubic YBCO-variant with a lattice parameter of 0.51 nm in c-YBCO/plasma-treated-YBCO/c-YBCO structure [8], while Wen et al. proposed that the modified interface in YBCO ramp-edge junctions has a kind of Ba-based perovskite-like structure, $(Y_{1-x}Cu_x)$-BaO_y with $x < 0.5$ [7]. This suggests that, under different experimental conditions and geometry of the samples, the structures of the interface barriers are likely different.

In order to develop more reliable fabrication procedures, it is necessary to study how the microstructure of the barrier varies with the experimental conditions such as the ion accelerating voltage and the atmosphere. Recently, Ishimaru et al., found a variation in RHEED patterns from the recrystallized a-axis YBCO interface, which was plasma-treated under different conditions. The results suggest a significant change in the micro-

structure of the recrystallized interface. In this paper, we report the detailed results on microstructural study of YBCO/plasma-treated YBCO/a-axis YBCO trilayer samples by transmission electron microscopy (TEM).

2. Experimental

a-axis oriented YBCO thin films were prepared on $SrTiO_3$ (100) substrate by pulsed laser deposition. A KrF excimer laser ($\lambda = 248$ nm) with a power density of about 2 J/cm² on a stoichiometric high-density target and a repetition rate of 5 Hz was used. About 200 nm thick films were grown in an oxygen pressure of 200 mTorr at a substrate temperature of 580°C. Fig. 1 illustrates the fabrication conditions of the four samples studied in this paper. The experimental details were described in Ref. [9]. Briefly, an ECR source with a grid was
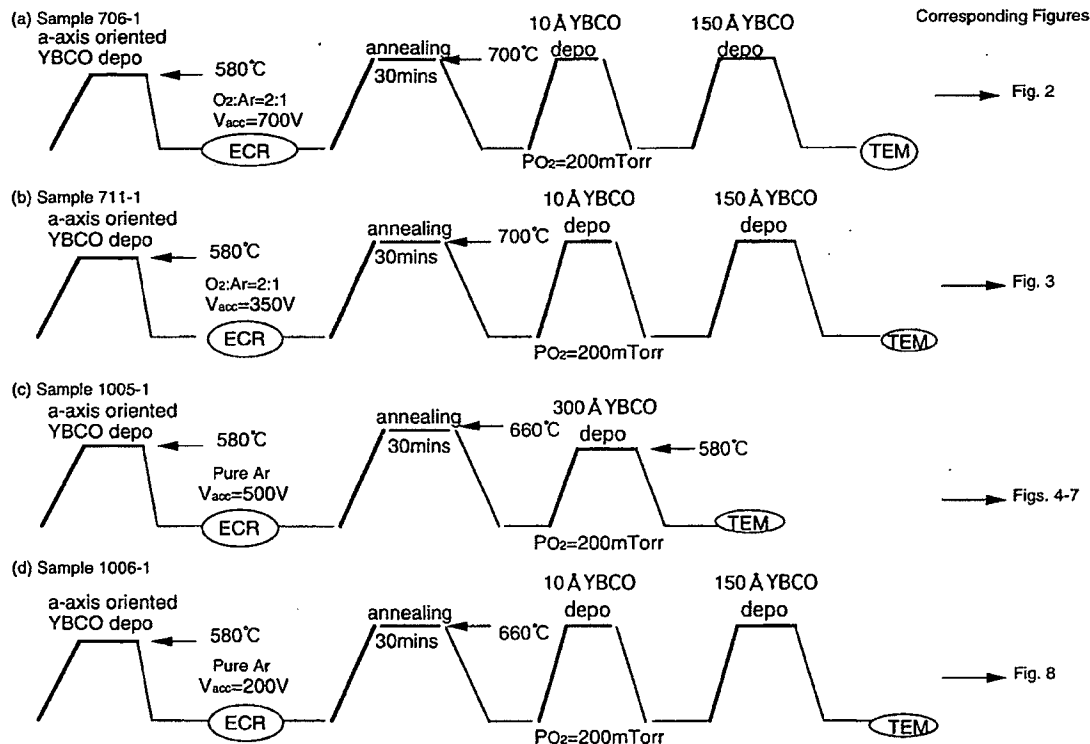
Fig. 1. Illustrations of the experimental procedures for the four samples examined.

used to modify the surfaces of a-axis YBCO films. Either pure Ar or Ar and O_2 mixed gas was employed and the accelerating voltage was varied between 200 and 700 V. In samples 706-1, 711-1 and 1006-1, we selected 700°C and 660°C as annealing temperatures and upper YBCO thin film deposition temperatures, respectively, because they were close to the temperature for making interface-modified barrier ramp-edge Josephson junctions in our group. In sample 1005-1, the upper YBCO thin film was deposited at a lower temperature (580°C) in order to avoid the presence of c-axis YBCO grains.

In order to protect the termination of the upper layer, which is easily damaged during the TEM preparation process, a layer of gold was deposited on the samples. Cross-section specimens for TEM were prepared by a standard method including mechanical grinding and ion-milling. TEM observation was carried out in a JEOL-4000EX operated at an accelerating voltage of 400 kV.

3. Results and discussion

Fig. 2 shows the cross-sectional TEM image of sample 706-1. The geometry of the sandwich structure is not what was intended: the upper YBCO layer consists of both a- and c-axis oriented

YBCO. It results from the high deposition temperature (700°C) for the upper YBCO film. No clear barrier material is observed between the upper and lower layer of YBCO, however, there is a 1–2 atom thick strained trace at the interface between the upper and lower a-axis YBCO, as indicated by black arrows in the inset, which is the enlarged image of the framed area. The difference in contrast around the interface area indicates the existence of strain field. The absence of secondary phases is consistent with the RHEED results reported in Ref. [9].

The detailed geometry of sample 711-1 is shown in Fig. 3(a). In some regions, a clear secondary phase – barrier layer is observed, as indicated by the arrows. The barrier layer grows on the a-axis YBCO with a cube-on-cube orientation relationship and is flat, uniform, strain-free, and thinner than 0.5 nm. Under the image condition employed, the Cu–O planes appear as white lines. It is evident that the Cu–O planes are interrupted by the thin barrier layer. However, the barrier layer did not cover the whole area of the lower YBCO, resulting in the connection of Cu–O planes in some other regions. The surface of a-axis film is not an ideally flat plane as well known and the thickness of recrystallized layer is less than 1 nm. Therefore, it is rather difficult to distinguish the intermediate layer from the lower and upper YBCO even in
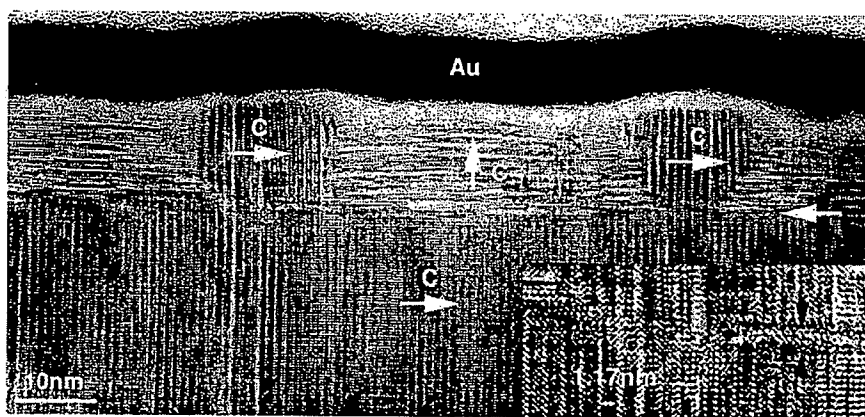
Fig. 2. Cross-section TEM image of a YBCO/plasma-treated YBCO/a-YBCO sample 706-1 which was treated under 700 V accelerating ion voltage and atmosphere of O_2:Ar = 2:1. The interface between the lower YBCO and the upper YBCO is indicated by the arrow. The enlarged image of the area in the frame are displayed in the inset.
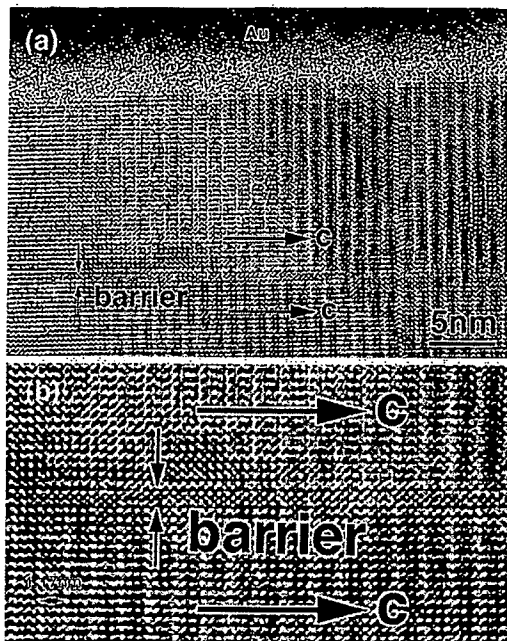
Fig. 3. (a) High resolution image of a YBCO/plasma-treated YBCO/a-YBCO sample 711-1 which was treated under a 350 V accelerating voltage and O_2:Ar = 2:1 annealing atmosphere. The interface between the lower YBCO and the upper YBCO is indicated by the arrow. (b) An enlarged image of the interface area in (a).

Fig. 4. Cross-section TEM image of sample 1005-1, in which the interface was formed by ECR treatment under a 500 V accelerating voltage in pure Ar annealing atmosphere and a lower deposition temperature for the upper YBCO layer.
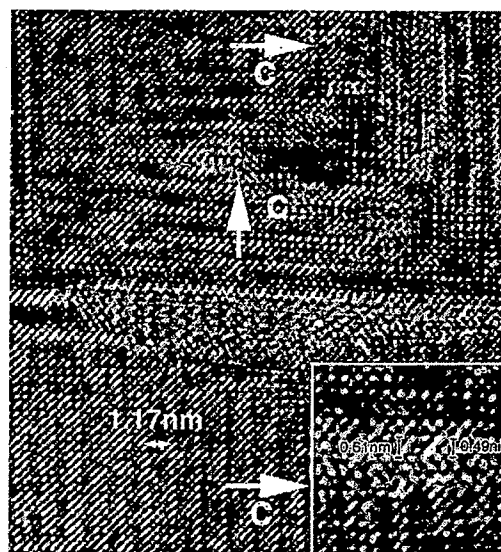
Fig. 5. High resolution image of one area of sample 1005-1 with an atomic configuration consisting of rectangles, in which the width is about 0.74 nm and length is about 0.52 nm. The inset is an enlarged image of the right side of the area.

an enlarged image shown in Fig. 3(b). However, a careful examination revealed a very small thickness variation of the barrier layer. Using the known a-axis YBCO lattice as a reference, the lattice parameter along the c-axis of the upper YBCO film is estimated to be 0.39 nm, while the lattice parameter along the a-axis ranged from 0.38 to 0.41 nm from place to place. This is in good agreement with the result reported in Ref. [8]. It suggests that there may be a slight composition variation in the barrier.

Fig. 4 shows a low magnification image of sample 1005-1. The barrier layer is clearly observed due to the existence of the strain contrast. Three kinds of microstructures of the ECR-treated interface layers were observed in the same specimen. HRTEM image in Fig. 5 shows that barrier layer can be about 2 nm thick. It is difficult to determine the composition of the barrier layer by EDX because a sufficiently strong signal could not

be obtained. However, d-spacings can be measured directly from the images using the adjacent YBCO fringes as a reference and identification of the phases in the barrier layer was made tentatively. The image configuration consists of rectangles, in which the length is about 0.74 nm and the width is about 0.53 nm. A careful checking of the X-ray database for all the compounds of Y, Ba, Cu and O reveals that the only possibility for the appearance of such atomic configuration is $BaCuO_2$, of which $d_{\{211\}} = 0.75$ nm, and $d_{\{222\}} = 0.53$ nm, respectively. The material on the left side of the barrier layer is so heavily strained that the atomic
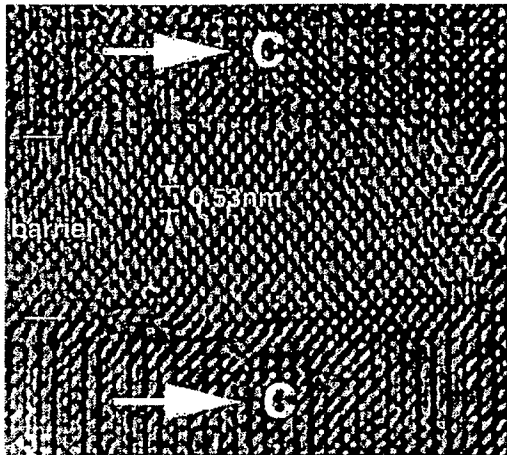
Fig. 6. High resolution image of another area of sample 1005-1. Here, the interface layer is about 4.5 nm thick and the atomic configuration consists of centered rectangles with the length of about 0.53 nm and the ratio of length to width ratio of about 1.4.
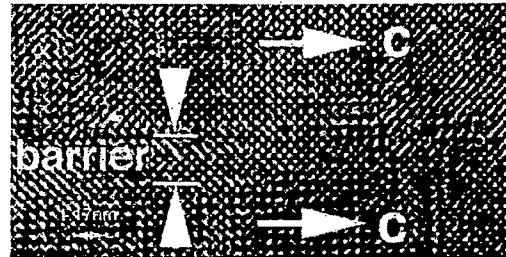

Fig. 7. High resolution image of the other area of sample 1005-1, showing an about 1 nm thick cubic structure similar to the one observed in Fig. 3.

configuration is invisible, while that on its right side is composed of centered rectangles with various lengths along the a–b planes, as shown in the enlarged image in the inset.

Another type of interface layer is shown in Fig. 6. The lattice image is similar to that reported by Huang et al. [7]. The image is considered to be taken from the [1 1 0] direction of cubic or pseudo-cubic structure, since the ratio of the length to the width of the centered rectangles in the image is approximately 1.4 and its lattice parameter is calculated to be about 0.53 nm. According to the X-ray database for the compounds consisting of Y, Ba, Cu and O, only Y_2O_3, of which the crystal structure is cubic with the lattice parameter $a = 1.06$ nm and the space group of Ia3, can give rise to such an atomic arrangement as shown in Fig. 6.

In the same specimen, a different atomic configuration was observed as shown in Fig. 7. This configuration appears to be similar to that shown in Fig. 3. Recently, Rutherford backscattering spectrometry (RBS) results indicated that the surfaces of the YBCO films, fabricated under the accelerating voltage of 350 V, are more Y-rich than those of the films treated under the accelerating voltage of 700 V [10], which is probably favorable for the formation of pseudo-cubic phases.

However, in pure Ar, the decomposition of YBCO may occur to some extent, which leads to the complicated structure of the interface.

In order to further clarify the effects of the accelerating voltage and the atmosphere on the microstructure of the interface, we investigated another sample 1006-1, as shown in Fig. 8. On the right side of the image, we observed two kinds of atomic configurations. It was found that one is the same as that in Fig. 5, i.e., $BaCuO_2$, and the other is the same as that in Fig. 6, i.e., Y_2O_3. Though the secondary phases are the same as those found in sample 1005-1, the interface layer in sample 1006-1 is strain-free. Both samples 1005-1 and 1006-1 were treated in Pure Ar, but at different accelerating voltages. This confirms that strain-free interfaces are formed at lower accelerating voltages.

None of the four samples examined displays full-coverage by the barrier materials. This may be due to both the large lattice mismatch between YBCO and the barrier layer, which leads to
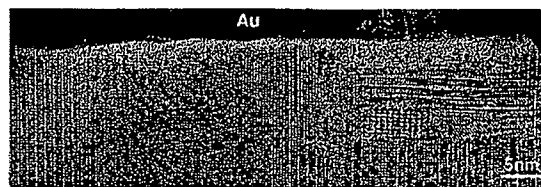
Fig. 8. TEM image of sample 1006-1, in which the interface was formed by ECR treatment under a 200 V accelerating ion voltage in pure Ar annealing atmosphere and lower deposition temperature for the upper YBCO. The presence of $BaCuO_2$ and Y_2O_3 is noticed along the interface at the right side of the image.

island-growth mode of the barrier layer during the initial growth stage, and the atomic-scale steps at the surface of the lower YBCO.

4. Conclusions

a-YBCO/plasma-treated-YBCO/*a*-YBCO 'tri-layer' thin films fabricated under different plasma-treatment conditions have been observed by TEM. The results show that

1. The interface under high accelerating voltage (700 or 500 V) is a strained one, while strain-free interfaces are formed under lower accelerating voltage (350 or 200 V).
2. A cubic barrier material with $a = 0.38$–0.41 nm and $c = 0.39$ nm is formed at the interface under the accelerating voltage lower than 500 V, while no secondary phase is observed under 700 V.
3. Plasma-treatment in pure Ar may result in the decomposition of YBCO to form Y_2O_3 and $BaCuO_2$ to some extent, while the treatment in Ar and O_2 mixture seems to suppress the decomposition.

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Current transport in ramp-type junctions with engineered interface

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The transport properties of "interface-engineered" edge-type $YBa_2Cu_3O_7$ Josephson junctions are investigated in detail. We have investigated the dependence of the current–voltage characteristics on external magnetic field, temperature, and microwave irradiation and compare them to the resistively shunted junction model. The temperature dependence of the critical current and the normal resistance allows us to draw conclusions to the transport of quasiparticles and Cooper pairs in the investigated "interface-engineered" junctions. We have studied the properties of junctions for which La doped $YBa_2Cu_3O_7$ is used for the superconducting electrodes. We will propose a model for the undoped and the La doped case which takes into account a barrier which consists of a series connection of a normal conducting layer and an insulator, containing superconducting microconstrictions. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1351056]

I. INTRODUCTION

Interface-engineered junctions (IEJs) are an interesting approach for the realization of reliable, controllable, high-temperature superconducting (HTS) Josephson junctions. The idea of fabricating a barrier by interface treatments instead of using an epitaxially grown nonsuperconducting thin film was first suggested by Moeckly et al.[1] At present, several groups are employing IEJs by using different approaches for the interface treatment.[2-7] All approaches have in common an ion treatment of the surface of the base electrode in the ramp area and a subsequent annealing step, but the methods for the generation of the ions and the process parameters differ strongly from group to group. However, each group claims that the junctions are much more reliable than ramp-type junctions with epitaxially deposited barrier layers, previously fabricated in their laboratories.

Since IEJs are resistively shunted junctions the most suitable model to describe their transport properties is the resistively and capacitively shunted junction (RCSJ) model.[8] For most cryoelectronic applications, e.g., superconducting quantum interference devices, digital circuits, or voltage calibrators, RSCJ-like junctions are required. Nevertheless, no detailed comparisons of the static and dynamic properties of IEJs to the RCSJ model at different temperatures have been published up to now.

The current transport and the nature of the barrier are still open questions since the results of microstructural investigations differ from group to group. Whereas some groups

observe the formation of a cation disordered (pseudo) cubic $YBa_2Cu_3O_7$(YBCO) phase,[9,10] Wen et al.[11] report on the formation of a Cu deficient YBCO phase $Y_{1-x}BaCu_xO_y$. There exists no consistent picture for the current transport. The published current densities, the normal resistances, and the suggested transport mechanisms differ for the junctions fabricated in different ways. Some groups observe properties of an insulating barrier containing localized states[4,5] whereas previous results of our group hint on a metallic behavior of the barrier material.[6]

The presence of La either in the superconducting electrodes or in the insulator strongly influences the properties of the junctions. Hunt et al. observed a strong increase of the normal resistance and a decrease of the critical current by using La doped YBCO for the bottom electrode.[2] Satoh et al. observed RCSJ-like current–voltage ($I-V$) characteristics only if La is present in the near area of the ramp.[5]

We will present detailed measurements of the transport properties of IEJs with $YBa_2Cu_3O_7$ (undoped junctions) as well as $YBa_{1.95}La_{0.05}Cu_3O_7$ electrodes [La(5%) doped junctions]. The $I-V$ characteristics as well as the dependence of the critical current I_C on external magnetic field, $I_C(H)$, were investigated for the whole temperature range below the superconducting transition temperature T_C. The $I-V$ characteristics and their response to microwave irradiation will be compared with the RCSJ model and the deviations will be discussed. We will propose a model to explain the transport of quasiparticles and Cooper pairs in undoped and La(5%) doped junctions and draw conclusions to the nature of the barrier.

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II. JUNCTION PREPARATION

The junction preparation process can be divided into the deposition of a YBCO–SrTiO$_3$ bilayer, the ramp fabrication process, the interface engineering, and the deposition of the counterelectrode.

First, a bilayer consisting of a 120 nm thick YBCO or YBa$_{1.95}$La$_{0.05}$Cu$_3$O$_7$ [La(5%) doped YBCO] film and a 220 nm thick SrTiO$_3$(STO) film is deposited *in situ* by pulsed laser deposition. We employed STO as well as LaAlO$_3$ as substrate materials and did not observe any influence on the film quality or junction properties. The YBCO films are deposited at a substrate temperature of $T = 805\,°C$, an oxygen pressure $p = 60$ Pa, an energy density of 2 J/cm^2, and a laser frequency of 10 Hz. The STO films deposited *in situ* on top of the YBCO films are fabricated at $T = 760\,°C$, $p = 15$ Pa, with the same energy density and frequency as for YBCO. Further details can be extracted from Ref. 12.

For the fabrication of the ramps, the bilayers are patterned by conventional photolithography. The STO film is Ar-ion-beam milled in a Kaufmann-type source using a current density of 0.25 mA/cm^2 and an energy of 250 eV. The sample is tilted 30° to the substrate normal and rotates during the etching process. The sample is cooled down to $-15\,°C$ during ion beam etching. The photoresist is then removed in an oxygen plasma. Subsequently, using the STO ramp as an etching mask, the YBCO ramps are ion-beam milled at the same etching parameters. This process results in ramps with edge angles of 20° for STO and 30° for YBCO. The thickness of the STO layer is reduced to 20–50 nm during the ion milling of the YBCO ramp. A more detailed description of the ramp fabrication process can be found in Refs. 12 and 13.

The interface engineering consists of a short *ex situ* ion-milling step at higher voltages and an annealing step in the deposition chamber. We investigated the parameters for these steps in combination with the deposition temperature of the counterelectrode using statistical methods.[12] In summary, we found out that the homogeneity of the junctions can be improved by using higher etching voltages and lower annealing temperatures whereas the critical currents of the junctions are mainly determined by the deposition temperature of the counterelectrode. Optimal junction properties are achieved by using a 5 min annealing step at 1200 V, a 30 min annealing step at 500 °C at the deposition pressure of 60 Pa O$_2$, and a deposition temperature of 760 °C for the counterelectrode.

The junctions with bridge widths between 1 and 8 μm are patterned by conventional photolithography and Ar-ion-beam milling. Finally, a 200 nm thick gold layer is evaporated and patterned by a lift-off process to provide electrical contacts.

Several undoped and La(5%) doped junctions were investigated by transmission electron microscopy (TEM) and no significant difference between the microstructure of the junctions was observed. The TEM micrograph of a La(5%) doped junction is shown in Fig. 1. At the interface between the bottom YBCO electrode and the counterelectrode a region with a slightly different contrast can be identified. However, in higher resolution, as shown in the inset of Fig. 1, no
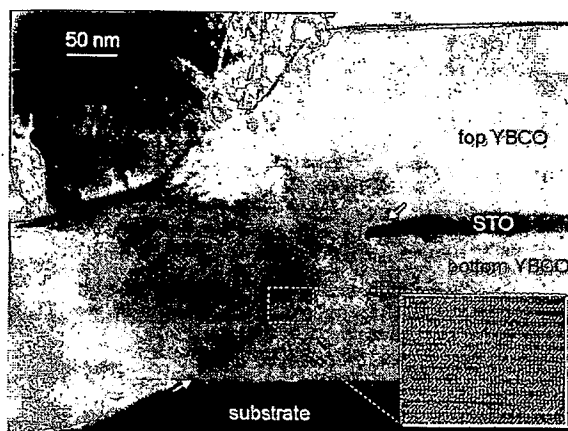

FIG. 1. TEM micrograph of the junction area. The arrows indicate the interface between the top and bottom electrode, which can be identified by a region with different contrast. The inset shows a high resolution image of the interface region. The thickness of the STO film is reduced to about 20 nm during the ion milling of the YBCO ramp.

interface layer with a different crystalline structure can be observed. This is in contradiction to the observations published in Refs. 9 and 11, where a 2 to 3 nm thin interface layer with a clearly different crystal structure was detected.

Cation disorder in the interface region due to the Ar-ion treatment could lead to local strain which may become visible in TEM as a region with different contrast. So the TEM investigations of our junctions are consistent with an interface layer where the orthorhombic crystal structure of YBCO is maintained, but in which some cation disorder is present.

III. STATIONARY PROPERTIES

The chip layout used for our investigations contains 40 junctions with 2–4 μm junction width. We investigated about ten chips with undoped junctions and about ten chips with La doped junctions with different La content. Since our process ensures the reliable fabrication of Josephson junctions, the measurements presented in this article are representative of our IEJs. The Josephson junctions are measured in the standard four-point geometry. A coil situated in our probe enables us to measure the $I–V$ characteristics in magnetic fields up to 3 mT. Trapping of flux is a crucial point in ramp-type junctions. Marx *et al.* showed by low-temperature-scanning-electron microscopy that magnetic flux is trapped in the YBCO film covering the ramp edge.[14] Therefore the junctions are shielded against external magnetic fields by Cryoperm shielding. Since self-generated fields also induce trapped magnetic flux in the junctions, the maximum critical current is often obtained at nonzero magnetic fields. Therefore we adjusted the magnetic field towards the maximum of the critical current before we recorded the $I–V$ characteristics. A detailed investigation of the magnetic-field dependence of the $I–V$ characteristics of our junctions will be published elsewhere.

The normal resistance R_N is determined by the slope of the linear part of the $I–V$ characteristics at high bias currents where $V \gg I_c R_N$.
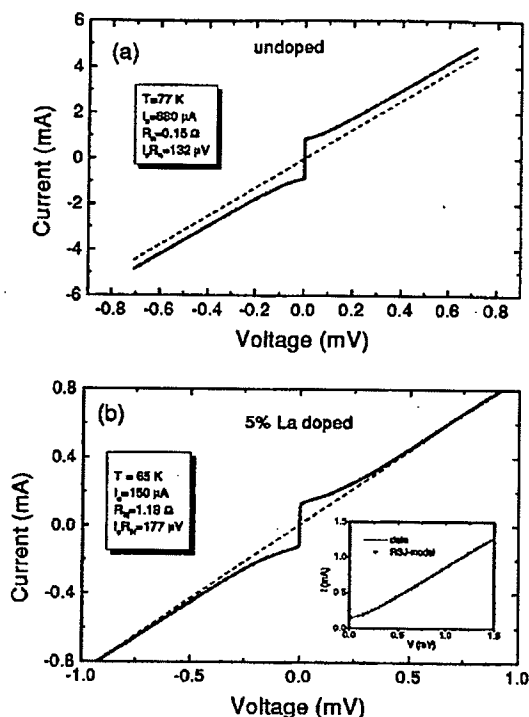
FIG. 2. (a) $I-V$ characteristic of a 4 μm wide undoped junction at 77 K. (b) $I-V$ characteristic of a 3 μm wide La(5%) doped junction at 65 K.

A. Influence of La doping on the junction properties

Figure 2(a) shows a typical $I-V$ characteristic of an undoped junction at 77 K. The parameters can be extracted from Table I. The shape of the $I-V$ characteristic is RCSJ-like but approximates at high bias current a straight line with a positive offset relative to the $I-V$ characteristic of an ohmic resistor [see the dashed line in Fig. 2(a)]. This offset corresponds to an excess current of about 500 μA.

For La(5%) doped junctions, supercurrents become detectable between 75 and 80 K although the critical temperatures of the La(5%) doped YBCO films are only slightly suppressed (at most 1 to 2 K). Figure 2(b) shows a typical $I-V$ characteristic of a La(5%) doped junction at 65 K. The shape can be well-described by the RCSJ model with neglected capacitance as can be seen in the inset of the figure.

The parameters of the undoped and the La(5%) doped junctions presented in Fig. 2 are summarized in Table I. It shows that the critical current density j_C of the La(5%) doped junctions is about one order of magnitude lower and

TABLE I. Summary of the junction parameters of the junctions in Fig. 2 (j_C: critical current density; $R_N A$: normal resistance times junction area; and T: measurement temperature).

Sample No.	La concentration	T(K)	j_C (A cm^{-2})	$R_N A$ (Ω cm^2)	$I_C R_N$(μV)
1	0%	77	1.8×10^5	7.2×10^{-10}	132
1	0%	65	2.5×10^5	6.2×10^{-10}	155
2	5%	65	4.2×10^4	4.2×10^{-9}	177

the $R_N A$ is about one order of magnitude higher than that for undoped junctions. Similar results have been obtained by other groups.[2]

Since a high concentration of La reduces the T_C of YBCO,[15] a possible explanation for the difference between undoped and La(5%) doped junctions could be that La diffuses into the ramp area and this agglomeration of La results in an interface layer with reduced T_C forming an additional barrier.

From this point of view, it seems possible to adjust the junction parameters by the La content. Therefore we investigated junctions fabricated with electrodes of doping levels from 0% to 7%. We identified two groups of junctions: For La(5%) and La(7%) doped junctions, the critical currents are about one order of magnitude lower and the normal resistances are about one order of magnitude higher than for the La(3%) doped and undoped junctions. This means that a threshold La content is needed to change the junction parameters, but it is impossible to continuously adjust the junction parameters. Due to these results, it seems unlikely that the La content itself determines the electrical properties of the barrier. However, La is prerequisite for the modification of the barrier layer.

To further investigate the role of La in the preparation process, we fabricated junctions where La(5%) doped YBCO was used either only for the base electrode or only for the counterelectrode. The junctions with La(5%) doped YBCO bottom electrodes behave like junctions in which both electrodes consist of La(5%) doped YBCO. The junctions with La(5%) doped YBCO top electrodes behave like undoped junctions. This shows that the interdiffusion of La is not the most important mechanism for the barrier formation in the La(5%) doped junctions because interdiffusion would as well occur during the fabrication of the counterelectrode. We conclude that La has to be present during etching and annealing to influence the formation of the barrier.

Hunt *et al.*[2] suggest that during the treatment of the ramp, the La atoms interchange in the interface region with a much higher probability with Y than Ba atoms, because the atomic radius of La is more similar to Y as the atomic radius of Ba. Wen *et al.* observed by TEM that if they utilize the La containing insulator ($La_{0.3}Sr_{0.7}$)($Al_{0.65}Ta_{0.35}$)O_3 the barrier is continuous whereas for $SrTiO_3$ a high number density of pinholes is observed.[11]

We did not observe a difference between undoped and La(5%) doped junctions by TEM. The nature of the barrier for the different types of junctions will be discussed in the context of the transport properties of our junctions in Sec. V.

B. Behavior of the junctions in different current density regions

Due to the increase of the critical current with decreasing temperature the short-junction limit where self-field effects of the critical current can be neglected may be exceeded at lower temperatures. Therefore we measured $I-V$ characteristics and $I_C(H)$ patterns for several samples for different temperatures below T_C. To check the role of self-field effects due to Joseph-son currents in our junctions, we regard the relation of the junction width w to the Josephson penetra-

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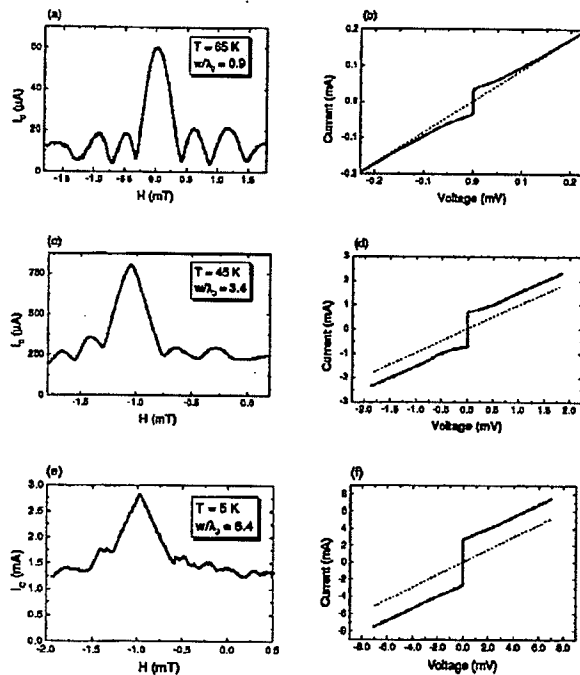
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FIG. 3. $I_C(H)$ patterns and $I-V$ characteristics of a 3 μm wide La(5%) doped junction at different temperatures: (a) and (b): 65 K; (c) and (d): 45 K; (e) and (f): 5 K. The dashed lines correspond to the Ohmic law with the respective R_N of the junction.

FIG. 4. Temperature dependences of w/λ_J for a 4 μm wide undoped junction and a 3 μm wide La(5%) doped junction. The dotted horizontal lines indicate the w/λ_J ranges where different shapes of the $I-V$ characteristics are observed in the junctions.

tion depth $\lambda_J = \sqrt{\hbar/2e\mu_0 d' j_C}$, with $d' = d + 2\lambda_L$ (see, e.g., Ref. 16). We used $d' = 2\lambda_{L,ab} = 300$ nm because supercurrents flow in the ab planes and the thickness of our barrier layer can be neglected ($\lambda_L/d \gg 1$ in any case).

Figure 3 shows the $I_C(H)$ patterns with corresponding $I-V$ characteristics of a 3 μm La(5%) doped junction at different current density regions. At 65 K, the critical current density is $j_C = 8.5 \times 10^3$ A/cm^2 corresponding to $w/\lambda_J = 0.9$. Therefore the junction is clearly in the short-junction limit. The $I_C(H)$ curve is very similar to the Fraunhofer pattern [see Fig. 3(a)]. Deviations from the ideal Fraunhofer pattern may be attributed to barrier inhomogeneities. The $I-V$ characteristic can be well-described by the RCSJ model and no significant amount of excess current is observed [see Fig. 3(b)].

At 45 K, the critical current density is $j_C = 1.1 \times 10^5$ A/cm^2 corresponding to $w/\lambda_J = 3.4$ which means that the junction is in the transition to the long-junction regime. There appears an excess current in the $I-V$ characteristics [see Fig. 3(d)] and the influence of self-field effects can be seen in the $I_C(H)$ curves: the second maxima are suppressed and the central maximum approaches a triangular shape [see Fig. 3(c)].

At 5 K, the current density is $j_C = 3.9 \times 10^5$ A/cm^2 corresponding to $w/\lambda_J = 6.4$. The long-junction characteristics are obvious in Figs. 3(e) and 3(f). The $I_C(H)$ characteristic is triangular, the second maxima are nearly completely suppressed as expected for a long junction.[16] Furthermore, there is almost 100% excess current in the $I-V$ characteristic [Fig. 3(f)]. The RCSJ model is not valid anymore.

Since barrier inhomogeneities may cause additional deviations from a homogeneous current distribution, there is no strict value of w/λ_J for which junctions switch from short junction to long junction behavior. Furthermore, although the ramp geometry is very similar to an overlap junction configuration, the electrodes are in the same plane and the boundary conditions may be different. Therefore a quantitative comparison of our $I_C(H)$ curves to existing calculations is not reasonable.

Nethertheless, some features of the junctions demonstrated in Fig. 3 are typical for all our junctions in the different j_C regions. At $w/\lambda_J \approx 4$, excess current becomes significant in the $I-V$ characteristics. Since undoped junctions and La(5%) doped junctions have different current densities, $w/\lambda_J = 4$ is obtained at different temperatures. To illustrate this effect, Fig. 4 shows the temperature dependence of w/λ_J for an undoped junction and a La(5%) doped junction. The temperature range can be divided into three regions of w/λ_J. For $w/\lambda_J > 4$, excess current becomes significant in the $I-V$ characteristics. For $w/\lambda_J > 11$, the $I-V$ characteristics have a positive curvature like flux-flow $I-V$ characteristics. In the case of La(5%) doped junctions, the junctions are RCSJ-like in the whole temperature range, but start to have a significant amount of excess current at 50 K. In the case of undoped junctions, the $I-V$ characteristics show ideal RCSJ behavior only in the vicinity of T_C. Below 55 K, the $I-V$ characteristics are already flux-flow-like. Therefore undoped junctions are not suitable for applications where ideal RCSJ behavior is needed at temperatures below 77 K.

Waldram *et al.* showed that for $w/\lambda_J > 4$ a dc supercurrent persists up to large voltages.[17] This supercurrent can be identified with our excess current I_{ex} because the voltage regime where the supercurrent should disappear is not obtained in the $I-V$ characteristics before dissipation in the superconducting electrodes leads to a positive curvature. The amount of additional supercurrent is expected to increase with increasing w/λ_J as experimentally observed in low-temperature-superconductor junctions.[17] Therefore it is reasonable to attribute the increase of the excess current in our junctions with w/λ_J to self-field effects. This is in agreement

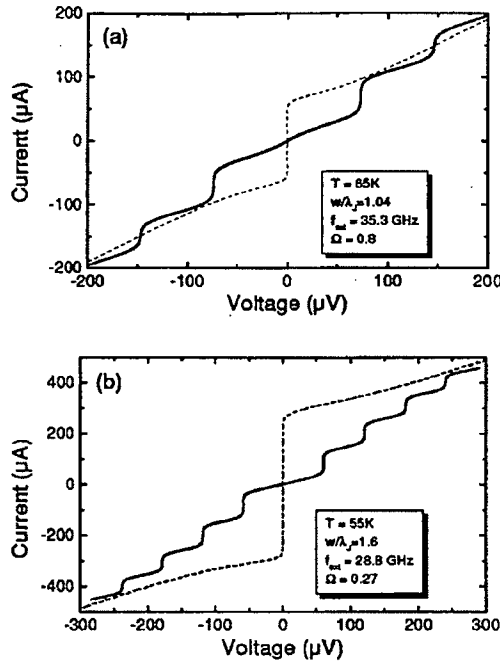3856   J. Appl. Phys., Vol. 89, No. 7, 1 April 2001

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FIG. 5. $I-V$ characteristics of a 3 μm wide La(5%) doped junction (a) at 65 K and (b) at 55 K. The dashed lines are the $I-V$ characteristics without microwave irradiation. The continuous lines correspond to the $I-V$ characteristics at (a) 35.3 GHz and (b) 28.8 GHz.

with the increase of I_{ex}/I_C with decreasing temperature which is observed in our junctions.

Concerning the observation of flux-flow-like $I-V$ characteristics at high current densities ($w/\lambda_J > 11$), heating effects as well as dissipation in the electrodes may be an explanation, especially at high temperatures. Furthermore, the T_C of a possible interlayer with reduced critical temperature may be exceeded in the corresponding temperature regime. However, it is not unreasonable to explain the observation of flux-flow-like $I-V$ characteristics with the dissipation of Josephson vortices in the junctions.

IV. DYNAMIC PROPERTIES

To compare the dynamic properties of our junctions with the RCSJ model at different characteristic frequencies $2eI_CR_N/h$, we investigated the $I-V$ characteristics of our junctions under microwave irradiation at two different temperatures. Since the La(5%) doped junctions are in the short-junction limit for a broader temperature range than the undoped junctions, we measured the microwave response of a La(5%) doped junction at 65 and 55 K.

Figure 5(a) shows the $I-V$ characteristics of a 3 μm wide junction with and without microwave irradiation at 65 K. With $w/\lambda_J = 1.04$, the junction is clearly in the short-junction regime and no significant excess current is visible. The $I-V$ characteristic exhibits well-defined Shapiro steps under microwave irradiation with a frequency f_{ext}. The characteristic voltage I_CR_N is 92 μV which results at $f_{ext} = 35.5$ GHz in a normalized frequency of $\Omega = hf_{ext}/2eI_CR_N = 0.8$.
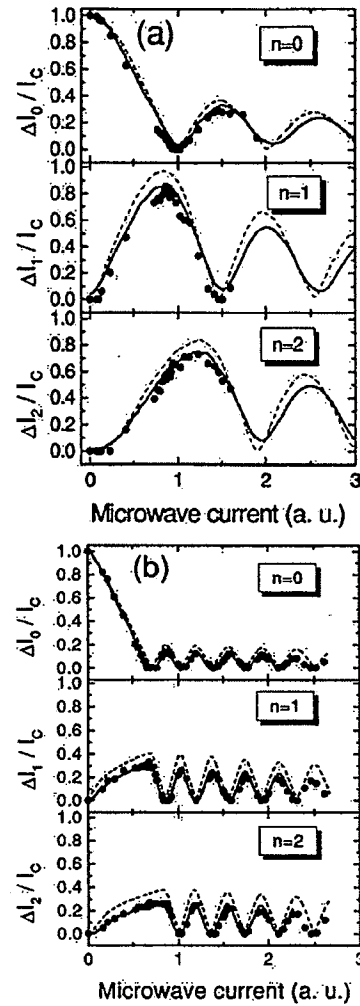
FIG. 6. Dependence of the Shapiro-step heights on the microwave current for $n=0,1,2$ of the junction shown in Fig. 4. (a) $T=65$ K and $f_{ext} = 35.3$ GHz. The dashed line shows the simulation without noise for $\Omega = 0.79$ and $\beta_C = 0.1$; the continuous line shows the simulation with noise parameter $\Gamma = 0.036$. (b) $T=55$ K and $f_{ext} = 28.8$ GHz. The dashed line shows the simulation without noise for $\Omega = 0.23$ and $\beta_C = 0.1$; the continuous line shows the simulation with noise parameter $\Gamma = 0.016$.

Figure 5(b) shows the $I-V$ characteristic of the junction with and without Shapiro steps at 55 K. With $w/\lambda_J = 1.6$, the junction is still in the short-junction regime, but some contribution of excess current to the critical current exists. The characteristic voltage I_CR_N is 270 μV which results at $f_{ext} = 28.8$ GHz in $\Omega = 0.27$.

Figure 6 shows the dependence of the heights of the Shapiro steps on the microwave current at 65 and 55 K. Additionally, in Fig. 6(a) the results of simulations with the RCSJ model with $\Omega = 0.79$ and $\beta_C = 2eI_CR_N^2C/\hbar = 0.1$ (C is the capacitance of the junction) without noise (dashed line) and with the influence of noise (straight line) are plotted. With a noise parameter $\Gamma = 0.036$, the data at 65 K can be well-described with the RCSJ model. At 65 K, the values for Ω and Γ correspond exactly to the values calculated from the

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measured $I_C R_N$ product and from thermal fluctuations, $\Gamma = 2ek_BT/\hbar I_C$, respectively.

In Fig. 6(b) the results of simulations with the RCSJ model with $\Omega = 0.23$ and $\beta_c = 0.1$ without noise (dashed line) and with the influence of thermal noise (straight line) are plotted. With a noise parameter $\Gamma = 0.016$, the data can be well-described with the RCSJ model. This value is higher than the noise parameter calculated from thermal fluctuations, $\Gamma = 0.009$, at 55 K. There is also a discrepancy between the $\Omega = 0.27$ determined from the static $I-V$ characteristics and the $\Omega = 0.23$ used for the simulation of the Shapiro steps at 55 K. Therefore at lower temperatures, the values for I_C and R_N determined from the static $I-V$ characteristics are not exactly suitable for the description of the dynamics of the junctions. A possible explanation is that with decreasing temperature additional transport channels influence I_C and R_N but do not contribute to the dynamics of the junctions.

For both investigated internal frequencies, corresponding to temperatures where the junction is in the short-junction regime, the dynamic properties qualitatively can be described with the RCSJ model. For lower temperatures, for which $w/\lambda_J > 4$, we observe subharmonic steps in the $I-V$ characteristics of this junction as predicted for Josephson junctions in the long-junction regime.[17]

V. CURRENT TRANSPORT PROPERTIES

The temperature dependencies of R_N and I_C allow one to draw conclusions to the transport of quasiparticles and Cooper pairs. Therefore we measured $R_N(T)$ and $I_C(T)$ for several undoped and La(5%) doped samples. In Sec. V A we present typical measurements of each junction type. In Sec. V B we propose a model which consistently explains the experimental results.

A. Temperature dependence of I_C and R_N

An important means to draw conclusions to the transport of quasiparticles is to investigate the temperature dependence of the normal resistance of the junctions. Figure 7(a) shows a typical temperature dependence of R_N for a 4 μm wide undoped junction. The resistance decreases with decreasing temperature from T_C to about 40 K as could be expected for a metallic barrier. Below 40 K, the resistance is temperature independent.

The typical temperature dependence of R_N of a La(5%) doped junction can be seen in Fig. 7(b). Similar to the case of undoped junctions, the resistance decreases with decreasing temperature for $T > 50$ K. Below 50 K, there is a striking difference to the undoped junctions, since R_N increases with decreasing temperature.

We analyzed the temperature dependence in the low-temperature regime in more detail. The temperature dependent contribution to the conductivity $\sigma(T) = 1/R_N(T) - 1/R_N(0\ \mathrm{K})$ against the temperature T in a double logarithmic plot can be seen in Fig. 8. In the temperature range from 0 to 50 K, the data points are on a line with the slope 4/3, resulting in

$$\sigma(T)(\Omega^{-1}) = 1/1.38 + 8.1 \times 10^{-4}\ T^{4/3}.$$
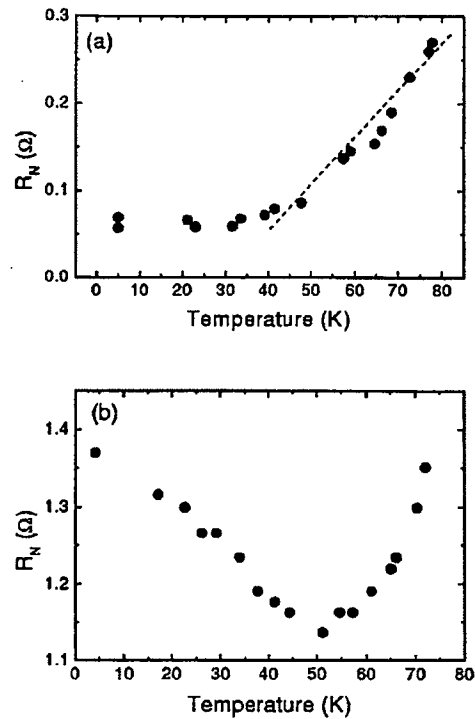
FIG. 7. Temperature dependence of the normal resistance (a) for a 4 μm wide undoped junction and (b) for a 3 μm wide La(5%) doped junction. The dashed line in (a) sketches the linear dependence of R_N between 80 and 40 K.

This behavior can be explained by the Glazman–Matveev theory.[18] Resonant tunneling via one and two localized states leads to the following dependence of I on V:

$$I = [\langle G_1\rangle + \langle G_2(T,0)\rangle + \langle G_2(0,V)\rangle] \cdot V, \tag{1}$$

$$\langle G_2(T,0)\rangle = A\ T^{4/3} \quad \text{for } eV \ll k_B T, \tag{2}$$

$$\langle G_2(0,V)\rangle = B\ V^{4/3} \quad \text{for } k_B T \ll eV. \tag{3}$$

The temperature and voltage independent part of the conductivity, G_1, contains the contributions from direct tunneling and tunneling via one localized state. The temperature
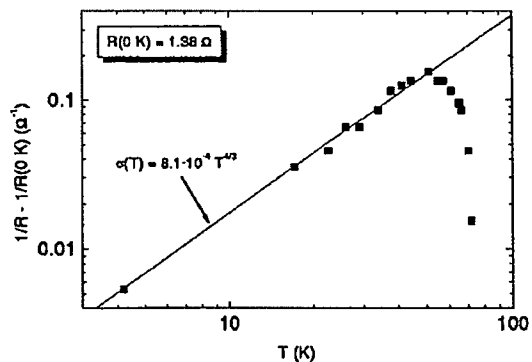

FIG. 8. Temperature dependent contribution to the conductivity of a 3 μm wide La(5%) doped junction in a double logarithmic scale. Straight line: Result of the linear regression of the data points from 0 to 50 K.

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and voltage dependent parts, $\langle G_2(T,0)\rangle$ and $\langle G_2(0,V)\rangle$, respectively, are contributions from resonant tunneling via two localized states. These voltage and temperature dependences have been observed for HTS junctions with different barrier materials, e.g., $PrBa_2Cu_3O_7$ (Refs. 19 and 20) and $SrRuO_3$.[21]

The voltage dependence of the normal resistance due to resonant tunneling via two localized states is expected to become visible for $eV > k_BT$ [see Eq. (3)]. In the case of junctions with $PrBa_2Cu_3O_7$ barriers, the voltage dependence was fitted to the Glazman–Matveev theory between 25 and 60 mV at 4.2 K.[20] In the case of our IEJs with a typical R_N of 1 Ω, this corresponds to currents of 25–60 mA, which are in the order of the current densities of the YBCO electrodes. Therefore for high bias currents we observe an increase of the resistivity due to dissipation in the electrodes which dominates a possible decreasing resistivity due to resonant tunneling via two localized states.

Summarizing, the normal resistances of undoped junctions decrease until they saturate at about 40 K. The normal resistances of La(5%) doped junctions as well decrease with decreasing temperature down to 50 K but start to increase with decreasing temperature below 40 K. The temperature dependence of R_N below 40 K can be explained by resonant tunneling via two localized states.

In order to draw conclusions to the transport of Cooper pairs we analyzed the temperature dependence of the critical current. Figure 9 shows typical $I_C(T)$ curves for an undoped [Fig. 9(a)] and a La(5%) doped junction [Fig. 9(b)]. The shapes of the curves are almost linear with an increase of the slope for low temperatures and near T_C. The characteristics cannot be fitted by an exponential law as expected for a superconductor–normal metal–superconductor (SNS) junction[22,23] and do not saturate at low temperatures as expected for a tunnel junction.[24] A so called "quasilinear" temperature dependence of the critical current, similar to our data, was observed for many HTS junctions.[25] For example, the $I_C(T)$ dependences of HTS junctions with Au interlayers were fitted to a superconductor–constriction–superconductor (ScS) model.[26]

For the undoped junctions, the interpretation of the $I_C(T)$ data is difficult because the $I–V$ characteristics are flux-flow-like below 60 K (see Fig. 4). Therefore for the main part of the temperature region below T_C, the critical current may be correlated with the pinning force of vortices and not with the Josephson-coupling energy. Due to these considerations, it is not reasonable to compare the $I_C(T)$ data of the undoped junctions with existing theories for Josephson junctions. Therefore for further analysis we regard only $I_C(T)$ curves of La(5%) junctions.

B. Model for the current transport

The temperature dependences of I_C and R_N of undoped and La(5%) doped junctions described in the previous section lead us to a consistent picture of the barrier for both types of junctions which is shown in Fig. 10. The barrier consists of a series connection of an insulator with pinholes (constrictions) and a superconductor with reduced $T_C(S')$. In the equivalent scheme in Fig. 10, it can be seen that there
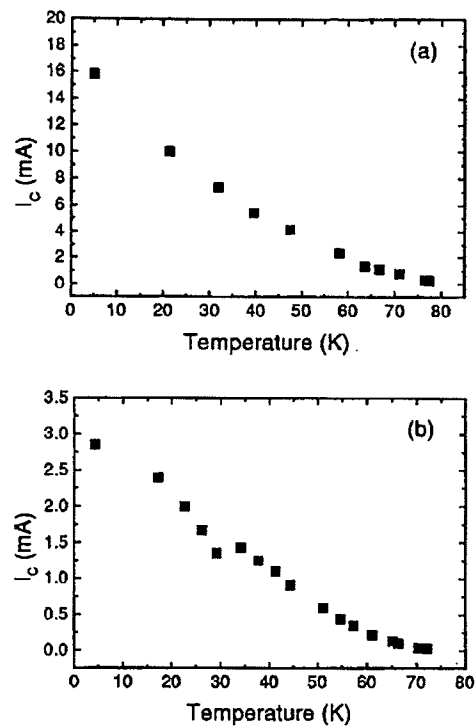

FIG. 9. Temperature dependence of the critical current (a) for a 4 μm wide undoped junction and (b) for a 3 μm wide La(5%) doped junction.

exist several channels in parallel in the insulating region ($R_0–R_2$ and R_{const}) and one metallic channel (R_{metal}) in the S' layer. The dominant channel in the insulating region depends on the density of constrictions, their diameter, the electrical properties, and the thickness of the insulator. Direct tunneling as well as resonant tunneling are transport mechanisms for the quasiparticles if the insulator contains localized states. Concerning the supercurrent, it is still an open question whether Cooper-pair transport via localized states is possible in HTS junctions or if pair breaking due to Coulomb
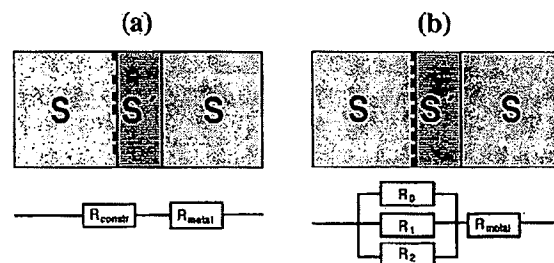

FIG. 10. Scheme of the barrier in the IEJs and equivalent scheme of the quasiparticle conductivity (a) for undoped junctions and (b) La(5%) doped junctions. The barrier consists of an insulator (black area) with pinholes (constrictions) and an S' layer. R_0: resistivity due to direct tunneling; R_1: resistivity due to resonant tunneling via one localized state; R_2: resistivity due to resonant tunneling via two localized states; R_{const}: boundary resistance in the constriction; and R_{metal}: resistivity of the S' layer above its T_C.

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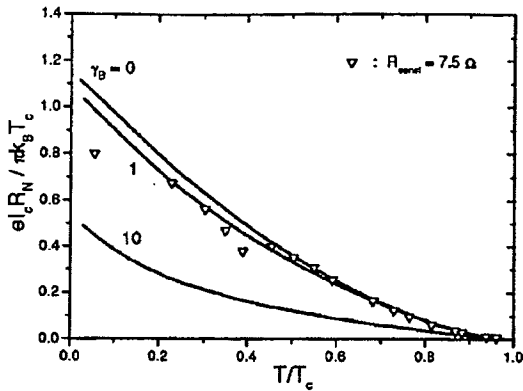
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FIG. 11. Comparison of the $I_C(T)$ data of a 3 μm wide La(5%) doped junction with the ScNS model (Ref. 28) Straight lines: Calculation of the normalized $I_C R_N$ in the ScNS model for $D=1$, $d_N/\xi=1$, $\gamma=1$, and γ_B =0,1,10. ∇: Normalized $I_C(T)R_N$ data with $R_{const}=5.7\,\Omega$ and $T_C=75$ K.

repulsion makes it impossible.[27] In our junctions, it is reasonable to assume that the Cooper-pair transport occurs via the constrictions in the insulator.

For the undoped junctions, no contribution from resonant tunneling via two localized states was observed. Therefore it is reasonable to assume that the density and the diameter of the constrictions allow Cooper-pair as well as quasiparticle transport through the constrictions. The resistivity of the constrictions is so low ($R_{const} \ll R_{0,1,2}$) that the current transport through the insulator can be neglected. At high temperatures, the normal resistance is determined by the resistivity of the S' layer, R_{metal}. Below 40 K, R_{const} exceeds R_{metal} and R_N is determined by the temperature independent interface resistance of the constrictions.

In the case of La(5%) doped junctions, the contribution from resonant tunneling via localized states to the quasiparticle transport can be observed in the temperature dependence of R_N (Fig. 8). This means that the diameter and the density of the constrictions are so small that the resistance of the constriction channels always exceeds the resistivity of the resonant-tunneling channels ($R_{const} \gg R_{0,1,2}$) [Fig. 11(b)].

The Cooper-pair transport occurs only via the constrictions. This enables us to compare the $I_C(T)$ data to calculations of a simplified model which describes the current transport through a series connection of a normal conducting N layer and a constriction (ScNS model).[28] Within this model, the NS sandwich is characterized by the suppression parameters γ, γ_B.[29] These parameters describe the proximity effect in the NS bilayer and are defined as

$$\gamma_B = \frac{R_B}{\rho_N \xi_N}, \quad \gamma = \frac{\rho_S \xi_S}{\rho_N \xi_N},$$

where R_B is the specific resistance of the NS interface, $\rho_{N,S}$ are the normal-state resistivities, and $\xi_{N,S}$ are the coherence lengths of the N and S materials, respectively. These parameters can be understood as follows: The parameter γ_B describes the effect of the boundary transparency between these layers. γ is a measure of the strength of the proximity effect between the N and S metals, i.e., it describes the diffusion of Cooper pairs from S into N across the interface. In our junc-

tions, a nonzero γ also describes that we do not have a sharp NS interface because the ion induced defects will decrease continuously in the superconductor at the interface which leads to a gradually increased order parameter. The constriction is characterized by the transmission coefficient D which accounts for the scattering of Cooper pairs in the constriction.

Figure 11 shows the normalized $I_C R_N$ product calculated for $\gamma=1$ and different values of γ_B. The transparency D is assumed to be $D=1$ because for $D<1$ the curves saturate at low temperatures what is not observed for our data. The shape is similar to the $I_C(T)$ curve of the La(5%) junction in Fig. 9(b). In order to compare our data quantitatively to the model, we would have to take the resistance of the constriction, R_{const}, which we are not able to extract from our experimental $R_N(T)$ data due to the existence of parallel conducting channels.

The open triangles in Fig. 11 show the normalized $I_C R_N$ product of the La(5%) doped junction if we choose R_{const} =5.7 Ω. The data fit well to the curve corresponding to γ =1 and γ_B=1. Similar agreement of our data could be obtained by comparing it to calculations with higher values of γ and γ_B which reduce the normalized $I_C R_N$ product. Because of the ambiguity of estimating R_{const} and the above-mentioned fact that the ScNS model only describes a sharp NS interface, it is not reasonable to make a quantitative fit and draw conclusions from the parameters. However, a qualitative agreement of our data to the ScNS model is obtained.

Furthermore, the ScNS model predicts an excess current in the $I-V$ characteristics due to Andreev reflections at the interfaces.[28] As mentioned in Sec. III B, due to self-field effects, a dc supercurrent exists which cannot be discriminated from an excess current due to Andreev reflections. Therefore it is not reasonable to discuss the existence of excess currents in terms of the ScNS model.

In summary, the model for our barrier sketched in Fig. 10 qualitatively describes the $R_N(T)$ dependence and the $I_C(T)$ dependence of the undoped and La(5%) doped junctions. Since we did not observe a material with different lattice constants at the interface in TEM studies, the layers with different electrical properties have to be identified with orthorhombic YBCO with different levels of damage. The fact that the properties of our junctions are stable in time and against O$_2$-annealing treatments suggests cation disorder instead of disorder in the oxygen sublattice to be the main lattice defect. Especially, the constrictions have to be identified with small areas with undisturbed YBCO in a cation disordered YBCO matrix.

It is difficult to distinguish between an N layer and an S' layer if an additional interface resistance is present, but it is more likely to attribute the metallic properties to an S' layer because YBCO becomes a disordered hopping insulator as soon as T_C is completely suppressed by the presence of defects. This would lead to a strong increase of R_N at low temperatures.

According to our model, the presence of La reduces the density and the diameter of the constrictions. That means that La homogenizes the engineered interface. This is partly

in agreement with the TEM investigations of Wen *et al.*[11] Although they detected a different barrier layer in their IEJs, they also observed a homogenization of their barrier in the presence of La.

VI. SUMMARY

IEJs have been fabricated by using $YBa_2Cu_3O_7$ as well as $YBa_{2-x}La_xCu_3O_7$ for the superconducting electrodes, and the role of La in our fabrication process has been investigated. The critical currents of the La(5%) doped junctions are about one order of magnitude lower as the critical currents of the undoped junctions, and the normal resistances are about one order of magnitude higher. We investigated different concentrations of La and found out that the properties of the junctions cannot be continuously adjusted by the La content, but there exists a threshold value of about 5% for La to influence the junction properties. This shows that La is prerequisite for the modification of the barrier but does not form the barrier by local doping of the interface.

At current densities where the junctions are in the small junction limit, the static $I-V$ characteristics as well as the $I-V$ characteristics under microwave irradiation can be well described with the RCSJ model. The $I_C(H)$ patterns in this regime are similar to the ideal Fraunhofer pattern. Junctions with w/λ_J in the order of 4 exhibit excess currents which can be attributed to self-field effects. In the case of the undoped junctions, the current densities are so high that ideal RCSJ behavior can only be observed near T_C. The La(5%) doped junctions are small junctions above about 50 K and are therefore more suitable for cryoelectronic applications.

The current transport in our junctions can be explained by a barrier consisting of a series connection of an S' layer and an insulator, containing microshorts (constrictions) and localized states. We suggest these layers and the constrictions to be YBCO with different degrees of cation disorder induced by the ion-milling treatment. For the undoped junctions, the resistance of the constrictions is so low that the quasiparticle transport as well as the Cooper-pair transport occurs via the constrictions in the insulator. The presence of La reduces the number density and the diameter of the constrictions. As a result, the quasiparticle-current transport in the La(5%) doped junctions occurs by resonant tunneling via localized states in the insulating layer. Since the $I_C(T)$ dependence can be fitted to an ScNS model, it is reasonable that the Cooper-pair transport occurs via the constrictions and not by resonant tunneling via localized states across the insulator.

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Recent Progress of High-Temperature Superconductor Josephson Junction Technology for Digital Circuit Applications

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SUMMARY   Recent progress of high-temperature superconductor Josephson junction technology is reviewed in the light of the future application to digital circuits. Among various types of Josephson junctions so far developed, ramp-edge-type junctions with a barrier layer composed of oxide materials in the vicinity of metal-insulator transition seem to offer a unique opportunity to fulfill all the requirements for digital circuit applications by virtue of their small junction dimensions, overdamped properties and relatively high I_cR_n product values at the temperature of around 30–40 K. Recently developed interface engineered junctions can be classified as junctions of this type. These junctions also raise an interesting problem in physics concerning the possibility of resonant tunneling of Cooper pairs via localized states in the barrier. From the viewpoint of practical applications, the improvement of the spread of the junction parameters is still a serious challenge to the present fabrication technology. Although interface engineered junctions seem to be most promising in this regard at present, 1σ spread of around 8% in the present fabrication technology is far from satisfactory for the fabrication of large-scale integrated circuits. The detailed understanding of the barrier formation mechanism in the interface engineered junction is indispensable not only for advancing this particular fabrication technology but also for improving other junction technology utilizing ramp-edge structures.

key words: *high-temperature superconductors, Josephson junction, SFQ circuit, ramp-edge-type structure, resonant tunneling*

1. Introduction

The development of superior-quality Josephson junctions with high I_cR_n product values is still one of the most important research issues relating to the electronics applications of high-temperature superconductors (HTS). Josephson junctions without hysteresis in their current-voltage characteristics are of particular importance in the construction of ultra-fast digital circuits utilizing a single flux quantum (SFQ) as an information carrier [1]. Among various types of Josephson junctions so far developed, ramp-edge type junctions with an artificial barrier layer schematically shown in Fig. 1 seem to be the most promising candidates for digital circuit applications because of their small dimensions, the potential controllability of junction critical current (I_c) and junction resistance (R_n) values, and the ease of superconducting wiring.

The operation of SFQ logic circuit is based on the transmission and storage of a single flux quantum by supercon-ducting loops which are connected either in series or in parallel. This operation principle results in the inductance L of the superconducting loops in SFQ circuits being restricted according to the inequality $0.5\Phi_0 < LI_c < 1.5\Phi_0$, where Φ_0 denotes the flux quantum $(=h/2e)$, and this limits the maximum I_c of Josephson junctions in practical circuits. Even if we adopt a superconducting ground plane technique utilizing c-axis oriented $YBa_2Cu_3O_{7-x}$ (YBCO) films with the London penetration depth of 0.2 μm, it would be difficult to reduce the inductance per unit square L_{sq} of a superconducting microstrip line to less than 0.6 pH. Since the minimum inductance of a practical loop in SFQ circuits is around 3–4 times L_{sq}, the maximum I_c value of a Josephson junction in the circuit should be less than 0.4–0.5 mA. On the other hand, for the reliable operation of an SFQ circuit, I_c must be sufficiently large compared with thermal and quantum fluctuation currents I_T and I_Q, where the fluctuation currents are defined as $I_T=(2\pi/\Phi_0)k_BT$ and $I_Q=(2\pi/\Phi_0)eI_cR_n$, respectively [2]. Thus the requirement that $I_c>>I_T$, I_Q restricts the maximum operation temperature of SFQ circuits as well as the maximum I_cR_n product value of Josephson junctions usable in a practical circuit.

Another restriction on the maximum I_cR_n product values of Josephson junctions in SFQ circuits arises from the fact that the McCumber-Stewart parameter β_c of a junction should be less than 1 to maintain overdamped characteristics [3]. The condition that $\beta_c<1$ is rewritten as $I_cR_n < \sqrt{\hbar/2eC}^{-1/2}I_c^{1/2}$, where C is the junction capacitance. This relationship is usually fulfilled automatically in junctions with a metallic barrier owing to its inherently small capacitance values. Unfortunately, however, it has been clarified that a high I_cR_n value cannot be expected for such junctions due to their extremely low junction resistance, as is discussed in the later section. Instead, recent interest has fo-
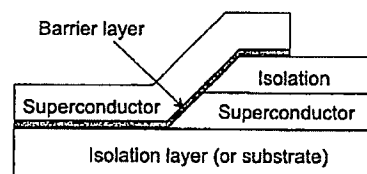
Fig. 1   Schematic representation of ramp-edge-type Josephson junction structure.

cused on junctions with an insulative barrier made of materials in the close vicinity of metal-insulator transition. In such junctions, resonant tunneling via localized states in the barrier is believed to play an important role in determining the junction characteristics [4]. However, the physical nature of the localized states in the barrier and its relevance to Josephson coupling have not been fully understood. Furthermore, there has been growing evidence that the charge transport across interfaces between electrodes and a barrier in a wide variety of junctions suffers from the localized states inevitably formed at the interfaces [5]–[8]. Proper understanding of the mechanism of current transport across a semi-insulative barrier has been one of key issues in the recent development of HTS Josephson junctions.

Another major challenge to HTS Josephson junctions is the uniformity of junction characteristics in a wafer and the reproducibility among wafers. The fabrication of SFQ circuits with reasonable yield requires a strict control of I_c values, say, less than 5% in the standard deviation of I_c for LSIs containing 1000 junctions [9]. Recently, some encouraging results, though not sufficient yet, have been reported for "interface engineered junctions" [10].

The intention of this paper is to review the recent progress of HTS Josephson junction technology for the future application to SFQ circuits operating at an elevated temperature. In this context, I focus on Josephson junctions with an artificial barrier layer and little discussion is given for grain boundary junctions in spite of their practical importance in SQUID applications and many common aspects of underlying junction physics [11].

2. Classification of HTS Josephson Junctions

In the past decade, a wide variety of materials with a resistivity ranging from 10^{-6} to 10^6 Ωcm have been tested as possible candidates for the barrier layer of HTS Josephson junctions, as shown in Fig. 2. It is known that a material can be classified either as a metal or an insulator depending on whether the material has a finite conductivity at zero temperature or not. The boundary between a metal and an insulator is given by the so-called "minimum metallic conductivity" σ_{min} [12].

In junctions with a metallic barrier, Josephson coupling between two superconducting electrodes originates from the penetration of Cooper pairs into the energy band of the barrier metal, which is known as the proximity effect [13]. Cooper pairs which penetrate into a normal metal can conserve their original phase in the superconducting electrode during the time interval given by $\tau \approx \hbar / k_B T$. Hence, the characteristic length scale ξ_n (normal coherence length) over which an appreciable amount of Cooper pairs exists is given either as $\xi_n = v_F \tau = \hbar v_F / k_B T$ (clean limit) or $\xi_n = \sqrt{D\tau} = \sqrt{\hbar D / k_B T}$ (dirty limit) depending on the electron mean-free-path in the normal metal, where v_F is the Fermi velocity and D denotes the electron diffusion constant. Due to the proximity effect, if the metal barrier thickness does not exceed several ξ_n, a finite number of Cooper pairs exist

throughout the barrier, resulting in a supercurrent flow between electrodes. ξ_n in Au at 4.2 K amounts to 100 nm whereas it decreases to less than 10 nm in Co-doped YBCO and in $(Sr,Ca)RuO_3$ at 70 K [14], [15]. Junctions which utilize the proximity effect to create a weak superconducting contact between electrodes are classified as SNS (Superconductor-Normal metal-Superconductor) junctions.

In junctions with a barrier having a resistivity larger than $1/\sigma_{min}$, Cooper pairs can transfer only by tunneling processes. In this sense, it is appropriate to classify all of these junctions as SIS (Superconductor-Insulator-Superconductor) junctions. The Josephson characteristics of an "ideal" SIS junction with a negligible amount of localized states in the barrier are fully understood. The weak superconducting contact in such a junction is established by direct tunneling of Cooper pairs between electrodes. The length scale which characterizes the barrier layer thickness to obtain a useful supercurrent density is determined by the penetration depth a of electron wave functions into the potential barrier, and is given as $a \approx \hbar / \sqrt{2mE_0}$ where m and E_0 are the electron effective mass and the potential barrier height, respectively. In the field of HTS junctions, $NdGaO_3$ and $PrGaO_3$ are thought to be promising candidates for the barrier layer in the "ideal" SIS junction because of their close lattice matching to YBCO [16], [17].

Insulators having a resistivity in the vicinity of $1/\sigma_{min}$ contain a large number of localized states in their bandgap and usually exhibit the variable range hopping conduction at low temperatures [12]. SIS junctions utilizing such a "dirty" insulator barrier show a complex behavior in their transport properties because not only direct tunneling but also resonant tunneling and hopping conduction via a finite number of localized states take place in the barrier layer [18]. The relative importance of each process depends on the barrier thickness, the radius and the density of the localized states, the temperature and the voltage across the electrodes. $PrBa_2Cu_3O_{7-x}$ (PBCO) and doped PBCO are typical examples of this type of barrier material [4], [19]–[22].

Further importance of the "dirty" insulator barrier in the field of HTS Josephson junction technology comes from the fact that high-temperature superconductors themselves lie in the close vicinity of the metal-insulator transition. This implies that an oxygen disorder, cation substitution, lattice dis-
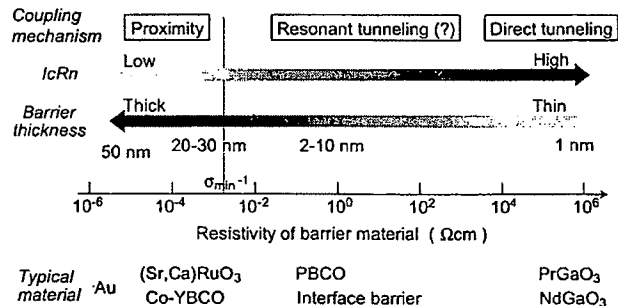

Fig. 2 Classification of high-temperature superconductor Josephson junctions from the viewpoint of the resistivity of the barrier material.

tortion due to stress and strain, or even a disruption of periodic lattice may result in the formation of a thin dirty insulator layer in high-temperature superconductors [6]. It is not difficult to suppose that such an insulator layer is apt to be formed at junction interfaces unless some care is taken to avoid it. In the rather early stage of HTS Josephson junction development, Gross has·pointed out that the barrier in grain boundary junctions has the nature of a dirty insulator [23]. Since then, there has been growing evidence that most of the HTS SNS junction characteristics suffer from the unintentional incorporation of an interface layer [7], [8].

In the following sections, we take a brief look at the representative junction characteristics of each type of HTS Josephson junction.

3. Josephson Junctions with a Metallic Oxide Barrier

The Josephson characteristics of an ideal SNS junction can be described by either the Eilenberger equations or the Usadel equations depending on whether the barrier material lies in the clean limit or in the dirty limit [13]. Although these equations can be solved numerically under appropriate boundary conditions which define the actual junction structure, it is not convenient to apply them directly to the analysis of experimental results. Fortunately, simple analytical formulae which describe I_c as functions of the barrier layer thickness and the temperature are known in some cases. In the case of an SNS junction in dirty limit, I_c at the temperature T not far from the critical temperature T_c of the superconducting electrodes can be described as

$$I_c = \frac{1}{R_n} \frac{\pi \Delta^2}{4ek_B T} \sum_{n \geq 0} \frac{8}{\pi^2 (2n+1)^2} \frac{\ell_n}{\sinh \ell_n} ,$$

$$\ell_n = (2n+1)^{1/2} \frac{d}{\xi_n(T)} , \tag{1}$$

where d is the barrier layer thickness, Δ is the order parameter at the junction interface and ξ_n is the normal coherence length [13]. Equation (1) can be simplified further if the condition that $d \gg \xi_n(T)$ is fulfilled as

$$I_c = \frac{1}{R_n} \frac{4\Delta^2}{\pi e k_B T} \frac{d}{\xi_n} \exp\left(-\frac{d}{\xi_n}\right). \tag{2}$$

Equations (1) and (2) indicate that I_c of an ideal SNS Josephson junction in the dirty limit should exhibit a nearly exponential dependence on both the square root of temperature and the barrier layer thickness in a relatively wide range of temperature. Another feature of SNS junctions is that their normal resistance values are determined simply by the resistivity and the thickness of the barrier. Recently, Delin and Kleinsasser have pointed out that most of the HTS SNS Josephson junctions so far reported do not exhibit the temperature dependence of I_c predicted by the conventional proximity effect theory [24]. The only exceptions are junctions with Ca-doped YBCO [25] or Co-doped YBCO [14] barriers.

Other junctions with a barrier material including Au [26], (La,Sr)CoO₃[6], CaRuO₃ [27] and SrRuO₃ [7], [15] exhibit a quasi-linear temperature dependence of I_c and an anomalously large R_n value, which are apparently beyond the scope of the proximity effect theory. These junction characteristics resemble those of grain boundary junctions, suggesting that some interface layer which governs the junction properties is formed in the junctions.

Char and coworkers have argued that the interface layer originates from the oxygen disorder at the YBCO electrode surface due to stress created by the thermal expansion mismatch between YBCO and the barrier [6]. It is not difficult to suppose that a certain amount of oxygen disorder in YBCO leads to the localization of electrons, resulting in the formation of an insulative barrier. However, it should be pointed out that a thin insulator layer which gives a resistance of as low as 10^{-8} Ωcm^2, that is, the typical value of the resistance observed for the "anomalous SNS junctions," suppresses the proximity effect between the electrode and the metal barrier almost completely [5]. Therefore, if a junction with a metal barrier of around 10 nm in thickness contains such interface layers on both sides of the barrier, we can hardly expect any observable Josephson current to flow across the junction. It is highly probable that the interface layer in the actual "anomalous SNS junctions" is formed only at the interface of one side. This may require another explanation for the formation mechanism of the interface barrier.

The proper proximity effect has been observed for junctions with either a Ca-doped YBCO or Co-doped YBCO barrier [14], [25]. In these junctions, the junction resistance showed a reasonable agreement with the value calculated from the bulk resistivity of the barrier material and the junction geometry. Furthermore, the junction critical current was confirmed to be described well by Eq. (3).

$$I_c = \frac{1}{R_n} \frac{\pi \Delta(0)^2}{4ek_B T_c} \left(1 - \frac{T}{T_c}\right)^2 \frac{d/\xi_n(T)}{\sinh(d/\xi_n(T))}, \tag{3}$$

where $\Delta(0)$ is the BCS order parameter in YBCO electrodes at 0 K. Equation (3) is an approximation of Eq. (1) under the assumption that the superconductive wave function and its derivative are continuous at the electrode-barrier interfaces [28]. Based on the detailed comparison between the experiment and the theory, Antognazza et al. have derived the conclusion that junctions with a 14% Co-doped YBCO barrier can be classified as SNS junctions in the dirty limit and that the electron diffusion constant in the barrier is D=6.6 cm²/sec [14]. The consistency of experimental data for Co-doped YBCO barriers with lower doping level as well as for 30% Ca-doped YBCO barrier was less satisfactory . The reason has been ascribed to the erroneous application of the dirty limit theory to these junctions [25].

The work by Antognazza et al. has demonstrated that the Josephson characteristics of HTS SNS junctions without an interface layer can be described quantitatively by the conventional proximity effect theory. At the same time, this clarifies the limitation of HTS SNS junctions for SFQ circuit ap-

plications. It is straightforward to calculate $I_c R_n$ values using Eq. (3) together with the expression for the normal coherence length ξ_n in the dirty limit. The junction resistance in unit area is expressed by

$$R_n = \frac{d}{2e^2 N(0)D},\tag{4}$$

where $N(0)$ is the density of state per spin for electrons at the Fermi energy in the barrier. By choosing $N(0)$ and D to be 1×10^{21} eV^{-1}cm^{-3} and 6.6 cm^2/sec, Eq. (4) gives an R_n value close to those actually observed for 14% Co-doped YBCO barrier junctions.

Table 1 summarizes the calculated $I_c R_n$ and R_n values. Some junctions seem to exhibit a high $I_c R_n$ product value at low temperatures. However, when we look at the R_n values of these junctions, it becomes obvious that we cannot expect such high $I_c R_n$ values for SNS junctions. For example, if we use a 5-nm thick barrier, R_n is of the order of 10^{-10} Ωcm^2. In order to attain an $I_c R_n$ product of 1 mV, the junction critical current density J_c must be of the order of 10^7 A/cm^2, which is close to the critical current density of bulk superconductors. It is highly questionable that a junction with such a high critical current density maintains a sinusoidal current-phase relationship required for proper Josephson characteristics. Furthermore, for HTS SFQ circuit applications, the allowable maximum I_c of the junction is limited to below 0.4–0.5 mA. Even if we adopt a ramp-edge-type geometry, the area of a practical junction would amount to 2×10^{-9} cm^2 (1 μm in junction width and 200 nm in electrode thickness). These restrictions limit the J_c of a junction to less than 2–2.5$\times10^5$ A/cm^2. When we apply this criterion to the data listed in Table 1, only the hatched region remains. This simple consideration leads to the conclusion that we cannot expect $I_c R_n$ product values exceeding, say, 0.5 mV for ideal SNS junctions.

A possible way to overcome the low-resistance problem in SNS junctions might be an intentional incorporation of an insulative interface layer in the junctions. In this case, the metallic barrier layer is utilized only as a means to create the interface layer and as long as the barrier layer is thinner than the normal coherence length, it does not play an impor-

tant role in determining the junction characteristics except for reducing the order parameter at the interface. Hunt et al. have demonstrated this type of junction by replacing the YBCO base electrode material in 5-nm thick Co-doped YBCO barrier junctions with La-doped YBCO [29]. The average $I_c R_n$ product of 0.3 mV has been attained at 65 K. The spread of I_c in a chip was 13%, which was comparable to the value reported for the low-resistance junctions with a Co-doped YBCO barrier [30].

4. Josephson Junctions with an Insulative Barrier Close to the Metal-Insulator Transition

The absence of superconductivity and nonmetallic behavior in $PrBa_2Cu_3O_{7-x}$ (PBCO) make the material an attractive candidate for a barrier in Josephson junctions with YBCO electrodes. Pioneering work on Josephson junctions with a PBCO barrier was first reported by Barner et al. [31] Since then, a considerable number of attempts have been made to create reliable YBCO/PBCO/YBCO Josephson junctions as well as to understand the mechanism of Josephson coupling in them [19]–[22], [32]–[36]. In the early stage of the development, junctions with a PBCO barrier had often been regarded as SNS junctions and analyses based on the proximity effect theory were made to explain the mechanism of Josephson coupling through the relatively thick PBCO barrier layers amounting to several tens of nm [32], [34], [35]. These attempts, however, failed to provide a reasonable explanation, though there still remains some possibility that one-dimensional metallic path along the Cu-O chains or even a superconducting pocket might exist locally in some of the PBCO barriers [37], [38].

The possibility of resonant tunneling of Cooper pairs via localized states with an attractive interaction between electrons in a barrier was first pointed out by Halbritter as an alternative explanation for Josephson coupling in YBCO/PBCO/YBCO junctions [39]. This idea has been extended by Devyatov and Kupriyanov to the theoretical conclusion that the Josephson critical current due to resonant tunneling via localized states with negligible Coulomb repulsion should exhibit the barrier thickness dependence of $\exp(-2d/a)$ as long as the barrier thickness d is far larger than the decay length a of wave function (=the radius of the localized states) in the barrier [40]. Since the junction resistance due to resonant tunneling of quasiparticles obeys the relation $\exp(-d/a)$, this model can give a reasonable explanation for the scaling behavior of $I_c R_n$ with the square root of I_c, which has been observed generally for PBCO barrier junctions [41]. Unfortunately, however, the relation that $I_c \propto \exp(-2d/a)$ is exactly the same as that for Josephson current due to direct tunneling of Cooper pairs. Furthermore, Glazman and Matveev have shown that a similar relation is also valid for resonant tunneling of Cooper pairs via localized states with an infinite Coulomb repulsion energy [42]. Thus the Josephson coupling mechanism in YBCO/PBCO/YBCO junctions has not been fully identified and is often discussed rather controversially. Nevertheless, experimental evidence is accumulating that

Table 1 $I_c R_n$ product values (in mV) as a function of barrier thickness (d) and operation temperature (T) expected for HTS SNS Josephson junctions with an ideal junction interface.

d (nm)	T=10 K	T=30 K	T=45 K	T=60 K	T=70 K	R_n (Ωcm^2)
5	14.5	8.0	4.5	2.0	0.9	2.4×10^{-10}
10	14.1	7.5	4.0	1.7	0.7	4.7×10^{-10}
15	13.6	6.6	3.4	1.4	0.6	7.1×10^{-10}
20	12.9	5.7	2.7	1.0	0.4	9.5×10^{-10}
25	12.0	4.7	2.1	0.7	0.3	1.2×10^{-9}
30	11.0	3.8	1.5	0.5	0.2	1.4×10^{-9}

YBCO/PBCO/YBCO junction characteristics are governed completely by the charge transport via localized states in the barrier [19]–[22], [33], [36]. In the following, this problem is discussed in detail based on our own experimental results.

We have fabricated YBCO/7% Co-doped PBCO/YBCO junctions with a ramp-edge geometry. The ramp-edge structure was produced using a photoresist mask reflowed after patterning together with Ar ion milling with substrate rotation during etching. The resultant ramp edges had a taper of 20° independently of the edge orientation in a wafer. After etching, the samples were heated to the temperature for the barrier layer deposition by sputtering. An activated oxygen flux from an ECR plasma source was supplied during the heating process. The junction properties were extremely sensitive to a variation in the substrate temperature and the power supplied to the ECR plasma source. We found that junctions fabricated at relatively low temperatures of around 700°C exhibited clear Josephson characteristics even without the deposition of a Co-doped PBCO barrier, indicating that an interface barrier layer was formed naturally during the annealing process. The problem posed by this interface barrier is discussed in Sect. 6 in detail.

In contrast, junctions fabricated at temperatures of around 750°C under a high oxygen flux exhibited Josephson characteristics only when a Co-doped PBCO barrier ranging from 6 to 11 nm in thickness was inserted between two YBCO electrodes. Junctions with a thinner barrier showed flux-flow dominated behavior, which is probably due to the presence of microshorts within the barrier.

Figure 3 shows a set of current-voltage characteristics observed for a junction with a 7.5-nm thick barrier at various temperatures. The junction exhibited RSJ-like characteristics with a small excess current below 50 K, and weak hysteretic behavior was seen at low temperatures (≤10 K). The critical current (I_c) and the junction conductance (G_n) observed at 4.2 K for junctions of 4 μm in width are depicted in Figs. 4 and 5 as functions of the barrier layer thickness. Both I_c and

G_n exhibited a nearly exponential dependence on the barrier layer thickness, and the decay parameters determined from the linear regression lines in the figures were 0.59 and 0.96 nm, respectively. The experimental fact that the decay parameter for G_n is almost twice as large as that for I_c can be more clearly seen in the $I_c R_n$ versus I_c plot in Fig. 6. Although the spread of data is still large, an overall tendency can be observed for the $I_c R_n$ values to scale with the square root of I_c.

In order to obtain further insights into the transport processes in our junctions, we measured the temperature dependence of G_n with the barrier layer thickness as a parameter. The results are shown by open squares in Fig. 7. We found that the temperature dependence could be modeled closely
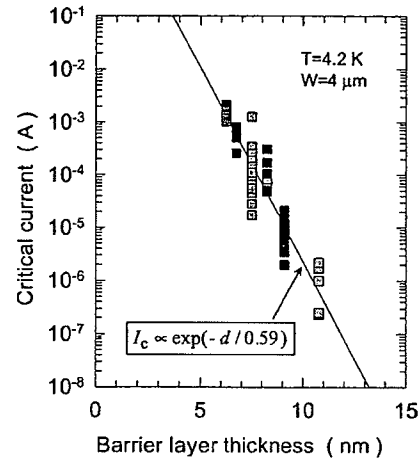
Fig. 4 Critical current versus barrier thickness observed for ramp-edge junctions with a Co-doped PBCO barrier. The decay parameter was estimated to be 0.59 nm from the linear regression line in the figure.

Fig. 3 Current-voltage characteristics observed for a ramp-edge-type Josephson junction with a 7.5-nm thick Co-doped PBCO barrier at various temperatures ranging from 5 to 50 K.
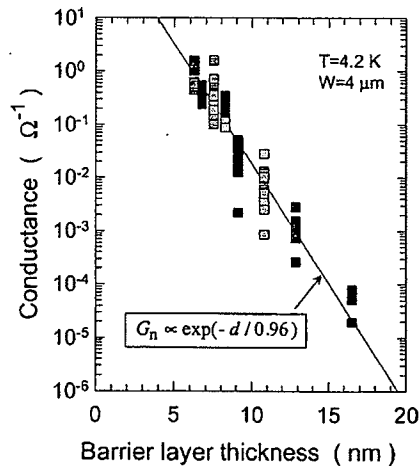
Fig. 5 Junction conductance versus barrier thickness observed for ramp-edge junctions with a Co-doped PBCO barrier. The decay parameter estimated from the linear regression line in the figure is 0.96 nm.

by the following formula:

$$G_n = G_0 + \alpha T^{4/3} + \beta T^{5/2} + \frac{\sigma_0}{d}\exp\left(-\left(\frac{T_0}{T}\right)^{1/4}\right) \quad (5)$$

where T is the temperature, d is the barrier thickness, and other symbols are fitting parameters. The first term in Eq. (5) represents the contribution of tunneling, whereas the second and the third terms correspond to hopping conduction through two and three localized states [18]. The last term denotes variable range hopping process via a large number of localized states. The solid lines in Fig. 7 represent the least-squares fit of the experimental data by Eq. (5). The agreement between the experiment and the calculation is satisfactory. From the fitting, we determined G_0 and α in Eq. (5) to be functions of d. We confirmed that α/d varied exponentially with d with a decay parameter of 1.4 nm. Theoretically, α/d is given as

Fig. 6 I_cR_n product versus critical current for junctions with a Co-doped PBCO barrier. The experimental data exhibit an overall tendency for the I_cR_n values to scale with the square root of I_c.

Fig. 7 Temperature dependence of junction conductance observed for junctions with a Co-doped PBCO barrier ranging from 6.25 nm to 16.5 nm. The solid lines are the least-squares fit by Eq. (5).

$$\alpha/d \propto \exp(-2d/3a) \quad (6)$$

where a is the radius of the localized states. The experimental result indicates that a is 0.93 nm. This value is very close to the decay parameter for G_0, indicating that G_0 in our junction is really dominated by resonant tunneling.

The experimental data suggest that the localized states in our Co-doped PBCO barrier is around 1 nm. This implies that the barrier height E_0 is about 38 meV. According to the recent study by Kakinuma and Fueki, high-temperature superconductors can be regarded as a kind of semiconductor doped with impurity, and the gap ΔE between the acceptor level and the top of the valence band becomes zero in YBCO with an oxygen content exceeding 6.5, whereas it remains finite in PBCO [43]. ΔE in PBCO is reported to range from 20 to 120 meV at 100 K depending on the oxygen content. These values are in reasonable agreement with our E_0.

The remaining problem is whether the Josephson current in our junction is consistent with the model based on resonant tunneling of Cooper pairs or not. Since the Coulomb repulsion energy between electrons at a localized states is expressed as $U \approx e^2/\varepsilon_r\varepsilon_0 a$, the value exceeds 160 meV even if we assume a large relative dielectric constant ε_r amounting to 100 in our Co-doped PBCO barrier. This value is far larger than any other energy scales relating to the resonant tunneling phenomenon in our junctions. Therefore, we adopted the theory given by Glazman and Matveev [42].

According to their theory, the possibility of resonant tunneling of Cooper pairs varies with the relation between two time scales: electron tunneling time $\tau_T = \hbar/\Gamma$ ($\Gamma = E_0\exp(-d/a)$) and the correlation time of the electrons in a Cooper pair $\tau_C = \hbar/k_BT_c$, where T_c denotes the transition temperature of superconductive electrodes. In the case of $\tau_T \gg \tau_C$, Coulomb repulsion U at the localized states results in a strong suppression of resonant Josephson current. The Josephson critical current at low temperatures under the condition of extremely large U is given as

$$I_c \approx (G_r/\pi e)E_0\left(d/a - \ln(E_0/\Delta)\right)\exp(-d/a) \quad (7)$$

where G_r is the junction conductance due to resonant tunneling and Δ is the superconducting gap energy. We calculated I_c as a function of d based on Eq. (7) by assuming that G_n in Fig. 5 was entirely due to resonant tunneling. The result corresponding to the regression line in Fig. 4 is shown in Fig. 8 together with the prediction by the direct tunneling model. The resonant tunneling model gives a satisfactory agreement with the experimental data. One difficulty in this model, however, is that we have to assume an extremely high density of localized states exceeding 10^{22} eV^{-1} cm^{-3} in order to account for the experimental G_n values. We have not found a reasonable solution to this problem, though the difference between the nominal and the actual barrier layer thickness due to the non-uniform growth of the barrier layer may be a possible explanation. At all events, it should be emphasized that our analysis is based on the theory which takes the large Coulomb repulsion at the localized states into account. We have
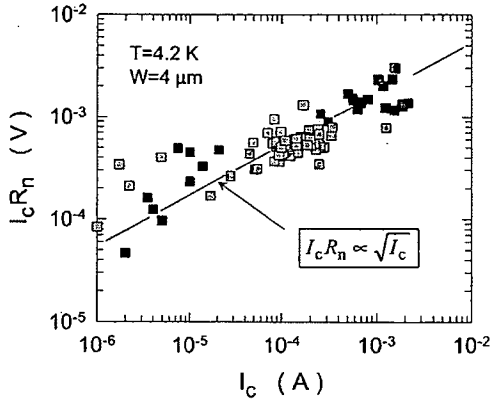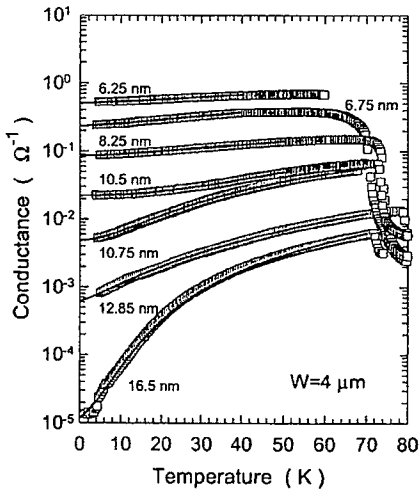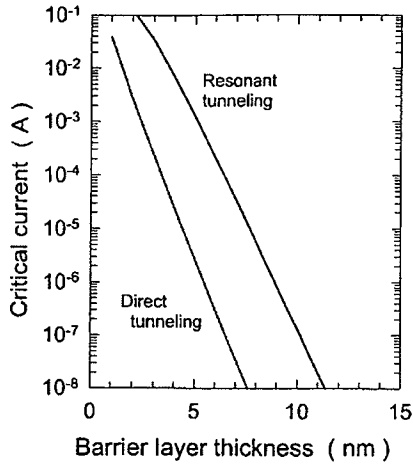
Fig. 8 Theoretical calculation of resonant Josephson current using Eq. (7) under the assumption that the experimental junction conductance shown in Fig. 5 is entirely due to resonant tunneling. The calculated result coincides well with the experimental I_c values shown in Fig. 4.

not found any experimental evidence that the localized states in PBCO possess an anomalous feature like a negative-U center as discussed by Halbritter [39].

The spread of I_c in our present Co-doped PBCO junctions is rather large: amounting to 35% in a chip. Though there is confidential evidence that we can reduce the value at least down to 10% by refining the process conditions [44], it is not clear whether we will be able to find a method to reduce the I_c spread further, say, down to a few % by the simple extension of the present technology. A serious challenge would be a complete step-flow growth of the barrier layer on the ramp edges to guarantee the uniformity in the barrier layer thickness.

5. Josephson Junctions with a Highly Resistive Barrier

The most successful Josephson junction technology in the field of low temperature superconductors is that based on Nb films and an AlO_x tunnel barrier of 1–1.5 nm in thickness. There are a few attempts to create SIS junctions similar to $Nb/AlO_x/Nb$ junctions in the field of HTS. The major difficulty with this approach lies in the fact that it requires an extremely thin barrier layer together with atomically smooth interfaces. Earlier attempts to use MgO [45] and $SrTiO_3$ [46] as the barrier were of limited success and recent interest seems to focus on other perovskite materials such as $NdGaO_3$ and $PrGaO_3$.

Grundler et al. have succeeded in fabricating YBCO ramp-edge-type Josephson junctions with a $NdGaO_3$ barrier layer having a nominal thickness of 2 nm [16]. The junctions exhibited current-voltage characteristics approximately coinciding with the resistively-shunted-junction (RSJ) model. Although the maximum I_cR_n product value of about 5 mV was attained at 4.2 K, the McCumber-Stewart parameter β_c

of the junction was rather small at around 13 at the critical current density of the order of 10^4 A/cm^2. The junction capacitance estimated from β_c was 0.15 μF/cm^2, which was more than one order of magnitude smaller than that expected for the 2-nm thick $NdGaO_3$ barrier layer. This small capacitance value together with the low junction resistance of around 3×10^{-7} Ωcm^2 cast a doubt as to whether we can really classify this junction as an SIS junction like a $Nb/AlO_x/Nb$ junction. There remains a possibility that the junction characteristics were not governed by the $NdGaO_3$ barrier itself but by some interface barrier which was formed unintentionally at the junction interface during the fabrication of the ramp-edge structure.

In order to remove the ambiguity concerning the junction interface, which arises more or less inherently in any ramp-edge-type junctions with an ion-milled surface, Tsuchiya et al. have developed $YBCO/PrGaO_3/YBCO$ trilayer junctions with a sandwich structure based on precisely controlled a-axis oriented YBCO films [17]. The junction with a 2.4 nm thick $PrGaO_3$ barrier exhibited a weakly hysteretic current-voltage characteristic ($\beta_c=3$) at 4.2 K and the critical current density and the normal resistance were 8×10^3 A/cm^2 and 3.5×10^{-7} Ωcm^2, respectively. These junction characteristics are similar to those observed for the ramp-edge-type junction with a $NdGaO_3$ barrier. It is difficult to imagine that an insulator such as $NdGaO_3$ or $PrGaO_3$ contains a high density of localized states as is definitely the case with PBCO. Apart from the fact that no indication of superconducting gap has ever been observed for these SIS junctions, which might be ascribed to the unconventional symmetry of order parameters in HTS, we have to seek a reasonable explanation for the low β_c values of the junctions originating from the anomalously low junction resistance and junction capacitance values.

6. Interface Engineered Junctions

A completely new approach to create an artificial barrier layer in ramp-edge-type junctions without the deposition of any barrier materials has recently been demonstrated by Moeckly and Char [10]. The basic idea is to create a thin layer of high-resistivity material on ramp edges by altering the structure or chemistry of the YBCO base electrodes only at the surfaces, which is a loose analogy of the tunnel barrier in $Nb/AlO_x/Nb$ junctions formed by oxidation.

The process to form an interface barrier originated by Moeckly and Char utilizes low-temperature annealing of YBCO ramp edges at 400–600°C in vacuum for 30 minutes followed by plasma treatment of the surface for several minutes in 10–100 mTorr Ar/O_2 mixture gas. The counter YBCO electrode is then deposited by laser ablation without breaking vacuum. Junctions fabricated by this rather simple process have exhibited clear Josephson characteristics coinciding well with the RSJ model, and the junction characteristics have been confirmed to be adjustable by varying the gas pressure and rf power during the plasma treatment. I_cR_n values ranging from 0.5 to 3 mV with corresponding R_n values of 6×10^{-8}–1.2×10^{-9} Ωcm^2 at 20 K have been reported. The most

significant feature of such interface engineered junctions is that they display a good uniformity in junction characteristics in spite of their relatively early stage of development. The 1σ spread in I_c of 7.8% and a spread in R_n of 3.5% over 10 junctions in a chip are far superior to those reported for any other junctions with an artificial barrier [47].

The high uniformity of the interface engineered junctions has been verified further by the subsequent work by Satoh and his co-workers [48], though the detail of their fabrication process differs considerably from that developed by Moeckly and Char. Satoh and his co-workers employed $(La_{0.3}Sr_{0.7})(Al_{0.65}Ta_{0.35})O_3$ (LSAT) as the substrate and the interlayer isolation material in the ramp-edge-type junctions. They found that a conventional ion-milling process to form the ramp-edge structure alone was sufficient to create an interface layer which acts as a barrier in Josephson junctions. A puzzling fact is that the junctions fabricated by the same process using $SrTiO_3$ as the substrate and the isolation layer material have not displayed Josephson characteristics. This experimental fact led them to the conclusion that a slight inclusion of La atoms at the interface during the ion-milling process enhanced the formation of the interface barrier layers. No evidence of this, however, has been verified yet. The spread in I_c of this new type of interface engineered junction is as low as $1\sigma=8\%$ for 100-junction array in a chip at 4.2 K.

The structure and the chemical composition of the barrier at the interface are still the subjects of intensive investigations [49]. Transmission electron microscopy (TEM) and microanalysis have revealed that a well-crystallized material with cubic or pseudo-cubic symmetry of around 2–3 nm in thickness covers the ramp-edge surfaces continuously without any detectable pinholes. The lattice parameter of the cubic or pseudo-cubic material, however, differs between junctions; it is 0.51 nm for the junctions by Moeckly and Char and 0.41–0.43 nm for the junctions by Satoh et al. [50]. Both of these lattice parameters are different from that of YBCO

with cubic symmetry which has previously been discovered to be formed on an ion-milled YBCO film surface after annealing [51]. Furthermore, it has been becoming evident that the chemical composition of the interface barrier layer differs considerably from that of stoichiometric YBCO [50]. Further investigation is definitely required to clarify the barrier layer formation mechanism.

Interface engineered junctions with a relatively large R_n value have exhibited a slight increase in R_n with decreasing temperature as well as a nonlinear behavior in their current-voltage characteristics at high voltages [10]. These features are similar to those observed for Josephson junctions with a PBCO barrier, indicating that the localized states in the barrier play some role in determining the junction properties. Figure 9 summarizes I_cR_n values of interface engineered junctions as functions of J_c reported by three independent research groups [47], [52], [53]. We can see an overall tendency that the I_cR_n values gradually increase with an increase in J_c at the region of relatively low J_c and then saturate at 2–3 mV in higher J_c. We can conceive two plausible explanations for such a behavior in the I_cR_n versus I_c characteristic.

One possibility is that the charge transport in the interface engineered junctions is governed entirely by resonant tunneling. In this case, as long as the barrier thickness is sufficiently large compared with the radius of the localized states, I_cR_n values vary with the square root of I_c, as discussed in Sect. 4. However, if the barrier thickness becomes sufficiently small to satisfy the condition τ_T (electron tunneling time) $\ll$ τ_C (correlation time of a Cooper pair), the probability that two electrons in a Cooper pair can tunnel through the barrier separately in time without the loss of the pair correlation increases [42]. In such a case, the Josephson current does not suffer a suppression due to the Coulomb repulsion, and the critical current can be expressed as

$$I_c = (\pi\Delta/2e)G_r . \qquad (8)$$

Comparison of Eqs. (7) and (8) shows that the relationship that $I_cR_n \propto \sqrt{I_c}$ changes to a new one in which $I_cR_n=$constant with decreasing the barrier layer thickness. The saturation behavior seen in the I_cR_n versus J_c plot may be an indication of this crossover in the barrier thickness dependence of resonant Josephson current.

An alternative explanation may be a crossover of transport mechanism from resonant tunneling to direct tunneling with a decrease in the barrier layer thickness. This type of crossover should accompany the change in the barrier thickness dependence of the junction conductance. Unfortunately, we do not have data to correlate the J_c and R_n values with the thickness of the interface barrier layer at present. In either case, we have to assume a reduced order parameter value at the junction interface in order to account for the experimental I_cR_n values.
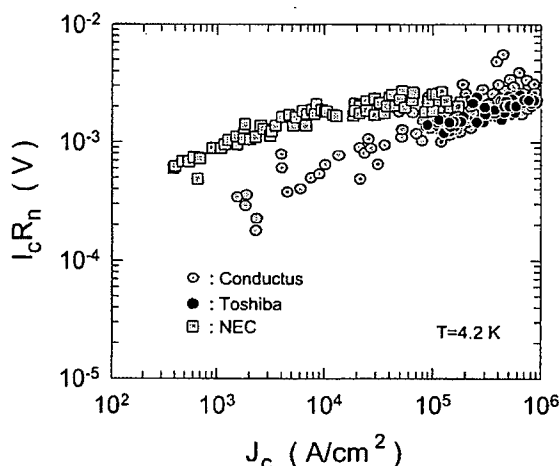

Fig. 9 I_cR_n product values of interface engineered junctions as a function of the critical current density observed by three independent research groups.

7. Conclusion

Recent progress in the fabrication technology and understand-

ing of junction physics has made it possible to design a realistic specification of HTS Josephson junctions for SFQ circuit applications. In HTS SFQ circuits, the maximum I_c value of the Josephson junction is restricted to around 0.4 mA. This corresponds to J_c of 2×10^5 A/cm^2 for 1-μm wide ramp-edge-type junctions with 200-nm thick superconducting electrodes. Such a J_c value has already been obtained in junctions with a PBCO barrier of around 6 nm in thickness as well as in interface engineered junctions, at least at 4.2 K. It is feasible to attain the same J_c value at higher temperatures, say, at 30–40 K, which may be a reasonable upper limit for operating SFQ circuits without a significant increase in the probability of thermally-induced bit errors.

The capacitance C in ramp-edge-type Josephson junctions has not been analyzed as fully as other device parameters such as J_c and R_n. For bulk PBCO, a relative dielectric constant of around 20 seems to be a good estimate [54]. If we adopt this value as a typical one in insulative oxides with a high density of localized states, the capacitance of a 5-nm thick PBCO barrier junction and that of an interface engineered junction with a 2-nm thick barrier are calculated to be 3.5×10^{-6} F/cm^2 and 8.7×10^{-6} F/cm^2, respectively. Only those junctions which fulfill the condition that the McCumber-Stewart parameter is less than one can be utilized in the construction of an SFQ circuit. This condition together with the J_c and C values estimated above determines the maximum $I_c R_n$ product of HTS Josephson junctions for SFQ circuit applications to be 2.7–4.3 mV. The performance of some interface engineered junctions has already been approaching these specifications.

The improvement of the spread of the junction parameters is a serious challenge to the present fabrication technology. Although interface engineered junctions seem to be most promising also in this regard, 1σ spread of around 8% in the present fabrication technology is still far from satisfactory for realizing HTS SFQ LSIs. The identification of the material composing the interface barrier and understanding of its formation mechanism are the most important issues and need to be addressed urgently.

The integration of Josephson junctions into SFQ circuits requires a multilayer process which can incorporate a superconducting ground plane to minimize circuit inductances. Several attempts have already been made to establish such a process and promising results indicating that the incorporation of a ground plane either underneath or over a Josephson junction does not affect the junction characteristics have been reported [55]–[58]. Further efforts, however, are definitely required to reduce the defects in the multilayers significantly compared with those at the present technological level in order to fabricate HTS SFQ LSIs with a reasonable yield.

Acknowledgment

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Atomic structure and composition of the barrier in the modified interface high-T_c Josephson junction studied by transmission electron microscopy

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The atomic structure and composition of modified interface junctions which showed reproducible critical current I_c ($I_c 1\sigma < 8\%$ for 100 junctions) are investigated by transmission electron microscopy. Transmission electron microscopic observations show the existence of a thin barrier (1–2 nm) homogeneously covering the ion milled edge of the base $YBa_2Cu_3O_y$ film although there is no barrier deposition and annealing process. High-resolution electron microscopy images and energy dispersive x-ray analysis with a spot size of 1 nm indicates that the barrier is a Ba-based perovskite-like structure, $(Y_{1-x}Cu_x)BaO_y$, with $x < 0.5$. A thin amorphous layer whose composition deviates from $YBa_2Cu_3O_y$ is formed due to the preferential sputtering of Cu. The amorphous layer recrystallizes into the nonequilibrium phase $(Y_{1-x}Cu_x)BaO_y$ after heating up to the deposition temperature. © *1999 American Institute of Physics.* [S0003-6951(99)02942-3]

Recently, interface-engineered $YBa_2Cu_3O_y$ (YBCO) junctions (IEJ), developed by Moeckly *et al.*[1,2] attracted much attention since the reproducible and manufacturable process of fabrication is quite suitable for digital circuit applications. In this process, no barrier deposition is carried out: the barrier is formed just by structural modification using ion bombardment and vacuum annealing. Recently, Satoh *et al.*[3] modified the process, in which the edge of the base YBCO film was formed by normal Ar ion milling and then the film was heated to a deposition temperature of about 700 °C in O_2 for a top YBCO layer deposition without being exposed to air. Their modified interface junctions (MIJ) also showed reproducible critical currents I_c, with a 1σ spread in I_c of less than 8% for 100 junctions.

In order to understand the formation mechanism of the barrier in these junctions, it is necessary to study the atomic structure and composition of the barrier by cross-sectional transmission electron microscopy (TEM), in particular, high-resolution electron microscopy (HREM) with nanometer-size element analysis. TEM investigations of Jia *et al.*[4] have shown that a homogeneous layer of a nonsuperconducting, cation-disordered cubic YBCO phase can recrystallize at an interface which is made amorphous by Ar ion-beam etching. Huang *et al.*[5] reported their TEM observations on the microstructures of IEJs and they concluded that the barrier is probably a cubic or pseudocubic YBCO variant. In this letter, the atomic structure and composition of the barrier in the MIJs are studied by TEM. We found that the barrier layer has a Ba-based perovskite-like atomic structure and composition, $(Y_{1-x}Cu_x)BaO_y$ with $x < 0.5$.

The base electrode YBCO layer and insulation layer $(La_{0.3}Sr_{0.7})(Al_{0.65}Ta_{0.35})O_y$, (LaSrAlTaO) (or $SrTiO_3$) were deposited on a LaSrAlTaO (or $SrTiO_3$) substrate by KrF pulsed laser deposition (PLD). In order to avoid the ion-milled YBCO edge being exposed to air prior to the top film

deposition, the insulation layer was first patterned by photoresist and then the YBCO edge was fabricated using the patterned insulation layer as a mask.[6] The 200 V Ar ion beam had an incidence angle of 30°–45° to the substrate surface. The fabricated edge was directly heated to about 700 °C without breaking vacuum for the further deposition of the top YBCO layer. This fabrication process has been described in detail elsewhere.[3,6] Cross-sectional specimens for TEM are mechanically ground by tripod directly down to a uniform thickness less than 10 μm and followed by an ion milling process. More details of the sample preparation can be found elsewhere.[7] Electron microscopy was performed with JEOL-4000EX and JEOL-2010 electron microscopes equipped with an Oxford energy dispersive x-ray (EDX) analysis system.

Two types of MIJs which exhibited resistively shunted junction (RSJ) and flux-flow (FF) type current–voltage ($I-V$) characteristics were selected to carry out TEM observations. The fabrication processes for these two types of junctions are similar; the only difference is that substrate and insulation layer are LaSrAlTaO for the RSJ type junction and $SrTiO_3$ for the FF type junction. Figure 1 shows a cross-sectional TEM image of a junction exhibiting RSJ $I-V$ characteristics. Although there was no barrier deposited, an interface can be clearly seen as a dark line in the low magnification image in the inset of Fig. 1. The structure of the barrier is different from YBCO, as indicated by white dashed lines in Fig. 1. CuO layers in YBCO films appear as white lines in this image, but these white lines cannot be observed in the barrier. The 2-nm-thick barrier covers the base YBCO edge homogeneously. The barrier consists of many small domains with a size of 2–3 nm. The orientations of different domains are more or less the same.

Figures 2(a) and 2(b) show HREM images of interfaces in MIJs exhibiting RSJ and FF type $I-V$ characteristics, re-
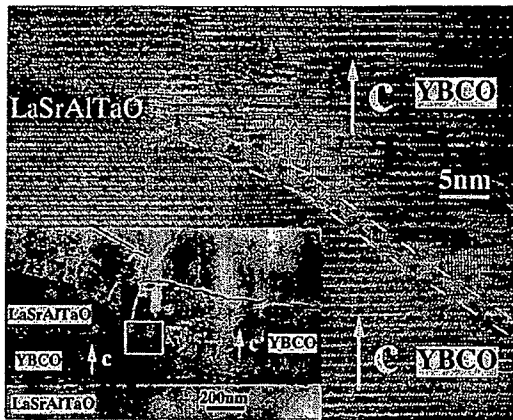
FIG. 1. Cross-sectional TEM image of a MIJ which had an RSJ type $I-V$ characteristic. The barrier (about 2 nm thick) is indicated by the dashed lines. Note the disappearance of CuO lines in the barrier. Inset is the low magnification image of junction.

spectively. In Fig. 2(a), although steps of height of 1.2 nm can be observed on the ion-milled surface, the 2-nm-thick barrier still fully covers the ion-milled surface. In contrast, one can see the continuity of CuO layers across the interface in the upper and lower part of Fig. 2(b). We believe this is the source of the FF type $I-V$ characteristics. The lattice parameters of the barriers in Fig. 2(a) and the circled regions in Fig. 2(b) are estimated to be about 4.1 Å along both the a and c axes of the YBCO film, using the lattice parameters of the YBCO film as an internal standard. In some areas of the barrier, one of lattice parameters along the c axis of the YBCO film is 4.3 Å, while the lattice parameter along the a axis of the YBCO film is still 4.1 Å as is shown in the inset of Fig. 2(a). Due to the slightly larger lattice parameter of the barrier compared to the YBCO films, one can observe misfit dislocations at the interfaces between the YBCO films and the barrier in Figs. 2(a) and 2(b).

High spatial resolution EDX analysis, with a probe size of about 1 nm, showed that the barriers in Figs. 2(a) and 2(b) have the same composition as each other but differ from YBCO, as shown in Fig. 3. The average atomic ratio of Y:Ba:Cu from 20 areas in the junction is 30:43:27. The EDX spectrum of the adjacent YBCO film (with known atomic ratio) was measured under the same conditions for internal calibration by the Cliff–Lorimer technique.[8] Compared to the YBCO film, Cu content is low in the barrier. This can be used to distinguish whether the electron beam is on the barrier or on the adjacent YBCO film by monitoring the intensity of the Cu peak during the EDX measurements. The atomic ratio Y:Ba in the barrier might be even higher, because some x rays from the adjacent YBCO may contribute to the EDX spectrum due to the comparable size of the electron beam and the barrier.

From the above results, one can see that the atomic structure and composition of the barrier material in MIJs exhibiting RSJ and FF type $I-V$ characteristics are similar. The only difference in microstructure is that the barrier fully covers the ion-milled edge in the RSJ type MIJs while the barrier does not fully cover the edge in the FF type MIJs. The RSJ type MIJs were made with LaSrAlTaO substrates and insulators and the existence of a small amount of La in
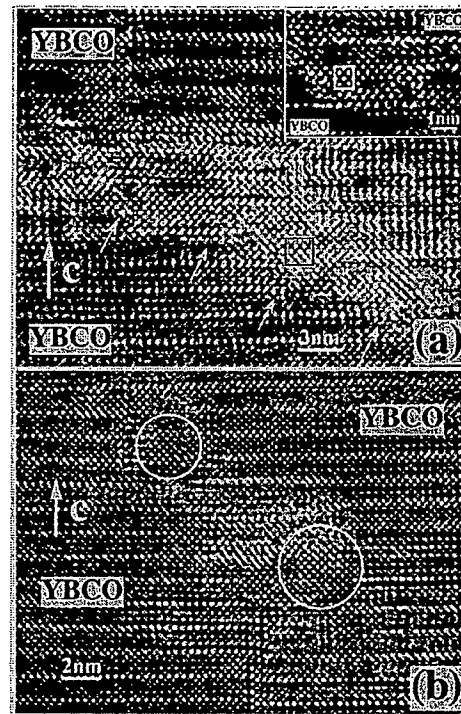
FIG. 2. HREM images of interfaces in MIJs exhibiting (a) RSJ type and (b) FF type $I-V$ characteristics. In most areas the lattice parameters of the barrier are 4.1×4.1 Å, while in some areas, one of lattice parameters along the c axis of YBCO film is 4.3 Å, as shown in the inset of (a). Steps on the bottom YBCO edge are indicated by small arrows in (a). Note that the continuity of CuO layers across the interface can be seen in the upper and lower part of (b).

the barrier due to redeposition during ion milling cannot be excluded. La may influence the coverage of the barrier, however, it was not found by EDX analysis. Another possible reason for the difference is that different substrates may slightly change the effective growth temperature, such that the coverage of the barrier is different. Recent experiments confirm that an RSJ type $I-V$ characteristic can also be obtained on a $SrTiO_3$ substrate with a $SrTiO_3$ insulation layer over a narrow range of deposition temperatures. The coverage of the barrier is more sensitive to the deposition temperature than La impurities.
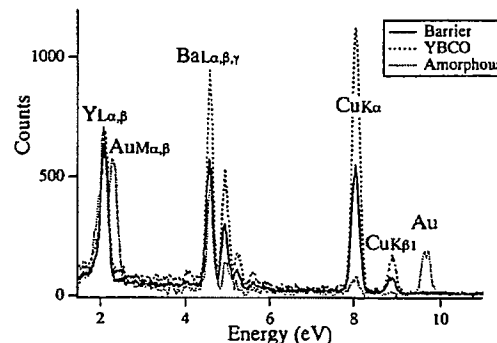

FIG. 3. EDX spectra of the barrier, the adjacent YBCO film, and the amorphous layer at circled regions in the inset of Fig. 4. The average atomic ratio of Y:Ba:Cu from 20 areas of the barrier is 30:43:27. The Cu content in the barrier is lower than that in the YBCO film.

From the HREM images and lattice parameters of the barrier shown in Fig. 2, the structure of the barrier is very possibly perovskite-like. All perovskite-like structures found in the YBCO system can be classified into two types according to the occupation rate at A or B sites in ABO_3. In the first type, Cu-based perovskite-like structures, Cu occupies the B site while Y and Ba occupy the A site. YBCO and cubic YBCO in which Y and Ba randomly occupy the A site are Cu-based perovskite-like structures.[4] The average lattice parameter of the Cu-based perovskite-like structure is about 3.9 Å. In the second type, Ba-based perovskite-like structures, Ba occupies the A site while Y and Cu occupy the B site. $(YCu_3)Ba_4O_y$ and $(Y_3Cu_5)Ba_8O_y$ are Ba-based perovskite-like structures.[9] The average lattice parameter of the Ba-based perovskite-like structure is about 4.1 Å, which is slightly larger than that of the Cu-based-like perovskite structure due to the large ionic radius of Ba. From HREM images, lattice parameters, and EDX analysis, one can conclude that the barrier is not a Cu-based, but a Ba-based perovskite-like structure. In all reported Ba-based perovskite-like phases, Y content is lower than Cu content. In the barrier it is the opposite, therefore, the barrier can be written as $(Y_{1-x}Cu_x)BaO_y$, with $x < 0.5$. This phase does not exist in the thermal equilibrium YBCO phase diagram. Kwestroo *et al.*[10] reported a perovskite-like $Y_2Ba_2O_5$ phase with lattice parameters of $a = b = 4.37$ Å, and $c = 11.85$ Å. The lattice parameters of the primary perovskite-like unit cell are then $a = b = 4.37$ Å and $c = 3.95$ Å. The barrier which shows lattice parameters of 4.1 Å × 4.3 Å could be a $Y_2Ba_2O_5$ phase, which contains nearly no Cu. Hence, the observation of 4.1 Å × 4.3 Å in some areas may indicate an inhomogeneous distribution of Cu in the barrier. Y_2O_3 phase (face-centered cubic, $a = 10.5$ Å) can be ruled out by the lattice parameters and the ratio of lattice parameters along the a and c axes of the YBCO film.[11]

In order to understand the composition change of the barrier which happened during the ion milling or heating process, we covered a freshly milled sample with an *in situ* Au layer. The Au layer was *in situ* deposited at room temperature by (PLD) to protect the surface from chemical or TEM sample preparation damage. Both substrate and insulation layer are $SrTiO_3$. Figure 4 shows a cross-sectional TEM image of the test sample. The thickness of the thin amorphous layer is about 1 nm, which is thinner than the barrier shown in Fig. 2(a). Note that the interface between the YBCO and the amorphous layer is quite smooth, as shown in Fig. 4, while the interface between the crystalline barrier layer and the bottom YBCO film shown in Fig. 2(a) is stepped. Both indicate a possible reaction might have occurred between the amorphous layer and the surface of the crystalline YBCO film during the heating process. EDX analysis on the amorphous layer shows a composition similar to the crystallized barrier, i.e., the Cu content is low. However, the exact composition is extremely difficult to estimate because x-ray scattering from the adjacent crystalline YBCO film cannot be avoided. At the bottom of the ion-milled edge, there is a small area in which only amorphous material exists between the Au and the $SrTiO_3$ substrate, shown in the inset of Fig. 4. EDX analysis at the spots indicated by circles in
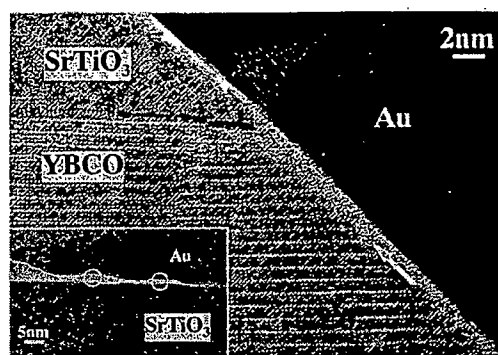

FIG. 4. Cross-sectional TEM image of a test sample in which the fresh ion-milled edge was covered *in situ* by an Au layer. A thin amorphous layer of about 1 nm can be seen on the YBCO edge. EDX measurements at the bottom of the ramp (circled regions) show that the Cu content in the amorphous region is nearly zero.

the inset of Fig. 4 shows that the atomic ratio of Y to Ba is close to 1, and the Cu content is nearly zero. So, we conclude that the composition deviation from YBCO is due to the preferential sputtering of Cu. This is consistent with the reported results that the sputtering yield of Y is about three times of that of Cu.[12–14]

In summary, we propose a formation mechanism of the barrier in the modified interface junctions which have no intentional barrier deposition or annealing process. A thin amorphous layer is formed on the edge of the ion-milled YBCO film whose composition deviates from YBCO due to the preferential sputtering of Cu. The barrier recrystallizes during the heating of the sample to the deposition temperature. The crystalline barrier is identified as a Ba-based perovskite-like structure, $(Y_{1-x}Cu_x)BaO_y$ with $x < 0.5$.

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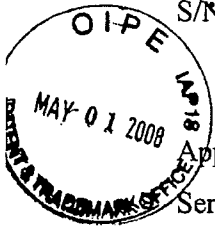[10] W. Kwestroo, H. A. M. van Hal, and C. Langereis, Mater. Res. Bull. 9, 1631 (1974).
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43USI2
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

CERTIFICATE UNDER 37 CFR 1.8:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail.Stop Amendment, Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 on April 28, 2008.

By __Carla J. Catalano__
Name: Carla J. Catalano

PETITION FOR EXTENSION OF TIME

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. §1.136(a), it is respectfully requested that a three-month extension of time be granted in which to respond to the communication mailed October 26, 2007, the period of response being extended from January 26, 2008 to April 26, 2008:

Payment is being made via credit card in the amount of $525 to cover the required fee for a small entity. Please charge any additional fees or credit any overpayment to Deposit Account. No. 13-2725.

Respectfully submitted,

23552
PATENT TRADEMARK OFFICE

MERCHANT & GOULD P.C.
P.O. Box 2903
Minneapolis, Minnesota 55402-0903
(612) 332-5300

Date: __April 28, 2008__

Tong Wu
Reg. No. 43,361   05/02/2008 SDENBOB3 00000003 10751091
TW:cjc   01 FC:2253   525.00 OP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MOECKLY	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket:	10467.43USI2
Confirmation No.:	2150	Due Date:	APRIL 26, 2008
Title:	HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

[stamp: MAY 0 1 2008]

CERTIFICATE UNDER 37 CFR 1.8:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on April 28, 2008.

By *Carla J Catalano*
Name: Carla J. Catalano

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

> **23552**
> PATENT TRADEMARK OFFICE

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment and Response (including attachments A, B and C)
- ☒ Request for Extension of Time for three-months and fee of $525
- ☒ Credit Card Payment Form (PTO-2038) in the amount of $525
- ☒ Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

Merchant & Gould P.C.	By: _____
P.O. Box 2903	Name: Tong Wu
Minneapolis, MN 55402-0903	Reg. No.: 43,361
612.332.5300	TWu/cjc

(PTO TRANSMITTAL - GENERAL)

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 10/751,091	Filing Date 01/02/2004	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒	OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =		X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	05/01/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 81	Minus	** 75	= 6	X $25 =	150	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 7	Minus	*** 6	= 1	X $105 =	105	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	255	OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/CORALIA BETANCOURT/

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 06/04/2008

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USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT A.5(a)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MOECKLY ET AL.	Examiner:	P. WARTALOWICZ
Serial No.:	10/751,091	Group Art Unit:	1793
Filed:	JANUARY 2, 2004	Docket No.:	10467.43US12
Title:	HIGH TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME		

DECLARATION OF JOHN M. ROWELL UNDER 37 C.F.R. 1.132

I, John M. Rowell, state and declare as follows:

1. I am a Research Professor in the School of Materials at the Arizona State University.

2. I hold a Ph.D. (1961), an M.A. (1961) and a B.A. (1957) in physics from Oxford University.

3. I joined Bell Laboratories in 1961 after carrying out my graduate studies at Oxford University. I held a series of management positions at Bell Laboratories and became Director of the Chemical Physics Laboratory in 1981.

4. In 1963, with P. W. Anderson, I made the first observation of the Josephson Effect and demonstrated the magnetic field sensitivity of the Josephson current. The observation was published in P. W. Anderson and J. M. Rowell, "Probable Observation of the Josephson Superconducting Tunneling Effect", *Phys. Rev. Lett.* 10, 230-232 (1963).

5. In 1966, I obtained what I believe to be the first patent (U.S. 3,281,609) granted for logic applications of the Josephson Effect.

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Attachment A

6. With W.L. McMillan, I developed tunneling spectroscopy, a measurement technique that determines in detail the electron-phonon interaction that causes superconductivity, at least in the low-Tc materials.

7. In collaboration with J. Geerk, M. Gurvitch and M. Washington, I invented the trilayer niobium/aluminum process that is now the basis of all low-Tc digital electronics and magnetic sensors.

8. In 1978, I received the Fritz London Memorial Low Temperature Physics Prize for this work on the Josephson Effect, tunneling and superconductivity.

9. In 1983, just prior to the divesture of the Bell System, I joined Bell Communications Research (Bellcore) as Assistant Vice President, Solid State Science and Technology. I was responsible for guiding the growth of this laboratory from its beginning, including both personnel and facilities. The technical programs of the laboratory included materials research, optoelectronics, optical switching, high speed electronics and high-Tc superconductivity.

10. In 1989, I joined Conductus, a start-up superconducting electronics company, as its Chief Technical Officer and served as its President for the year of 1991.

11. I have been a consultant specializing in applied superconductivity and the superconductor industry since 1995.

12. In 1997, I was appointed as the Materials Institute Professor at Northwestern University.

13. I have served on a number review boards and committees, including, for example, at the National Science Foundation, and have testified before Congress on research and technology funding issues.

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14. I am a Fellow of the American Physical Society, of the American Association for the Advancement of Science, and a Fellow of the Royal Society. I am a member of the National Academy of Sciences and of the National Academy of Engineering.

15. I have reviewed (a) the U.S. Patent Application Serial No. 10/751,091 ("the '091 application"); and (b) K. Harada, H. Myoren, and Y. Osaka, "Fabrication of all-high-Tc Josephson junction using as-grown YBa2Cu3Ox thin films," *Jap. J. Appl. Phys., vol. 30*, pp. L1387-89 (1991) ("the Harada paper").

16. With my experience as outlined above, I am familiar with the subject matters of the '091 application and the Harada paper.

17. The '091 application discloses a high-T_C Josephson junction in which a barrier between the two high-T_C superconductor layers is made by Argon-Oxygen ion-treatment of a thin surface layer of one of the superconductor layers and thus native to that superconductor layer. The ion treatment process disclosed in the illustrative embodiments in the '091 application resulted in a uniform, reproducible, high-quality barrier, as evidenced by the consistencies in the critical current (I_c) and normal resistance (R_n) values shown in Figure 6 of the '091 application and high values of the product I_cR_n (0.3 to 5 mV at 4.2K) for the Josephson junctions.

18. It should be noted that in the process disclosed in the illustrative embodiments of the '091 patent, the Ar-O ion-treatment step for forming the barrier layer is performed *in situ* following the formation of the edge surface of the first superconductor layer by Ar ion milling and annealing. *See*, the specification at page 11, lines 13 through 20. Therefore, one can be certain that the subsequent Ar-O ion-

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treatment step acts on a clean edge surface layer of the superconductor layer, and that the barrier is a modified layer of the superconductor layer.

19. The Harada paper reports a Josephson junction formed between two high-T_c superconductor layers. To form the junction, an insulating film of amorphous YSZ is deposited on the bottom superconductor layer. A portion of the insulating film is subsequently removed by the lift-off technique to expose a surface area of the bottom superconductor layer. The exposed area is then treated with an Ar-O plasma. The top superconductor layer is then deposited over the treated area. *See,* Figure 2 and associated text at page L1388 of the Harada paper.

20. Although the process reported in the Harada paper apparently resulted in a Josephson junction, the Josephson junction is of very poor quality, as evidence by an I_cR_n product of only 12μV, which is over an order of magnitude lower than disclosed in the '091 application. The Harada paper also does not demonstrate any reproducibility of the Josephson junction. Such a poor-quality Josephson junction could simply be due to a poor contact, or a contaminated interface, between the two superconductor layers and not necessarily a barrier that is an ion-modified surface layer of the bottom superconductor layer.

21. The statements in the paper are also ambiguous regarding the nature of the barrier: On the one hand, the paper contends that a barrier without grain boundary or insulating films was formed by the plasma treatment; on the other hand, the paper states that the "plasma treatment is very important since the surface layer of the base electrodes may be contaminated and/or have other nonsuperconducting phases." (p. L1388 of the Harada paper.) It is therefore not clear from the Harada paper whether the reported

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plasma treatment was intended to modify the bottom superconductor layer or merely to clean its surface.

22.   Furthermore, according to the Harada paper, the surface of base electrode is exposed using a "lift-off" technique. Because such techniques involve using solvents to dissolve the insulating layer and photoresist, the exposed surface is typically contaminated. It is therefore not clear that the plasma treatment reported in the Harada paper was acting on a clean surface of the superconductor. The Harada paper therefore does not necessarily show that the barrier was made of an ion modified surface layer of the superconductor layer.

23.   In sum, it is not clear from the Harada paper that a barrier made of an ion-modified surface layer of a high-T_c superconductor was produced. The Josephson junction reported in the Harada paper is significantly inferior to those disclosed in the '091 patent, and simply experimenting with the process reported by the Harada paper would not have lead to the Josephson junction disclosed in the '091 patent.

All statements made of my own knowledge are true, and all statements made on information and belief are believed to be true. Furthermore, I make these statement with the understanding that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and may jeopardize the validity of the application or any patent issuing thereon.

Dated: ___4\24\08___   ___John M. Rowell___
                                John M. Rowell

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USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT B.1

Fabrication of All-High-T_c Josephson Junction Using As-Grown YBa$_2$Cu$_3$O$_x$ Thin Films

Kanji HARADA, Hiroaki MYOREN[1] and Yukio OSAKA[1]

*Department of Electrical Engineering, Tsuyama National College of Technology,
624-1, Numa, Tsuyama 708*
[1]*Department of Electrical Engineering, Faculty of Engineering, Hiroshima University,
1-4-1, Kagamiyama, Higashi-Hiroshima 724*

All-high-T_c Josephson junctions consisting of a YBCO/barrier/YBCO-layered structure using epitaxial YBCO films sputtered on MgO(100) have been successfully fabricated. The barrier layer was obtained by Ar+O$_2$ plasma treatment of the surface of the base electrodes. These junctions show superconductor/normal-metal/superconductor (SNS)-like current-voltage characteristics. Constant-voltage current steps observed in response to 10 GHz microwave radiation show that ac-Josephson effects occur in these junctions.

KEYWORDS: YBa$_2$Cu$_3$O$_x$ thin films, deposited on MgO(100), all-high-T_c Josephson junction, plasma treatment, ac-Josephson effect

After the discovery of superconductivity above 77 K,[1] the possibility of fabricating a high-T_c Josephson junction stimulated substantial research efforts. The fabrication of reproducible junction of the high-T_c superconductor is the most important technology for device applications such as a Josephson computer, microwave mixer or SQUID sensor. Therefore, the thin-film-type Josephson junction has many advantages for practical applications because of the reproducibility of integration. To our knowledge, thin-film "tunnel junctions" have not yet been produced in high-T_c superconductors because of the small coherence length and severe interface degradation of the oxide superconductors. On the other hand, a number of techniques have been developed for the formation of "weak links" between high-T_c superconductors. The most commonly studied weak link is that which is formed naturally between two grains of a polycrystalline single-layer film.[2,3] However, there has been little success in the fabrication of reproducible Josephson junction. Recently, many efforts have been made to fabricate reproducible Josephson junctions such as artificial fabrication of a grain boundary junction on a SrTiO$_3$ bicrystal substrate,[4] YBCO/PrBCO/YBCO-layered junctions[5] and YBCO edge junctions.[6]

In this paper, we report on the successful fabrication of all-high-T_c Josephson junctions consisting of a YBCO/barrier/YBCO-layered structure using epitaxial YBCO films sputtered on MgO(100). The barrier layer was obtained by Ar+O$_2$ plasma treatment of the surface of the base electrodes without grain boundaries or insulating films.

A superconducting YBCO base and counter electrodes were deposited by RF magnetron sputtering. The target used was stoichiometric YBa$_2$Cu$_3$O$_x$ powder which was made by sintering at 900°C for 24 h in air. The substrate was electrically heated by the self-resistance of the Si substrate. As shown in Fig. 1, in order to achieve stoichiometry of the films sputtered on the substrate, we put the substrate at an off-centered position for the target. The substrate electrode was usually positively biased to provide a suitable amount of oxygen into the deposited films and protect the films from the bombard-

Table 1. Sputtering conditions of base YBCO and counter YBCO films.

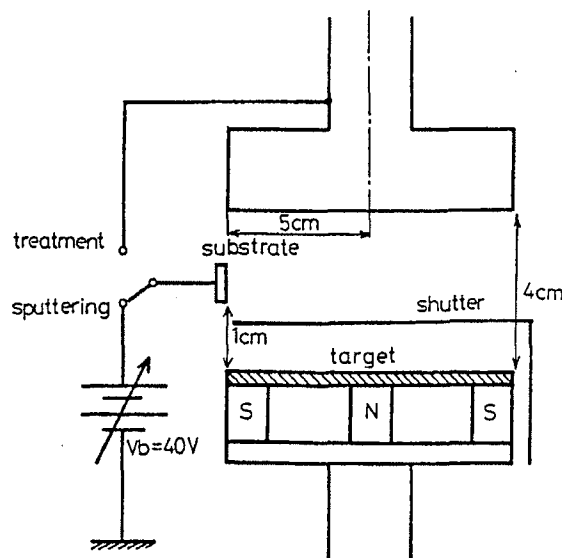|	
Target	YBa$_2$Cu$_3$O$_{7-x}$ powder
Target diameter	4 inches
Substrate	MgO(100)
Substrate temperature	700°C
Sputtering gas	Ar+O$_2$ Ar:O$_2$=2:1
Gas pressure	4 Pa
RF input power	140 W
Growth rate	5 nm/min

Fig. 1. Electrode and substrate geometry of the RF magnetron sputtering and treatment system used in this experiment. This substrate configuration avoids the bombardment of high-energy charged particles.

ment of the charged particles.

The schematic details of the junction fabrication process are shown in Fig. 2. The YBCO base electrodes in these junctions were deposited by sputtering on MgO(100) at substrate temperatures of about 700°C using an *in situ* process. The typical thickness was 100 nm. At the first step of this process, the base electrodes were lithographically patterned by the chemical etching technique. The chemical etchant was a 1% aqueous solution of phosphoric acid (Fig. 2(a)). Afterwards, the base electrodes were lithographically patterned and then covered by a thin insulating film of amorphous YSZ using electron beam evaporation (Fig. 2(b)). Using the lift-off method, the photoresist and the amorphous YSZ film on the junction were removed. And lift-off technique was used to open up on the area of the MgO(100), in order to the counter electrodes to grow epitaxial. Next, the barrier layer at the surface of the base electrodes was formed using the Ar+O₂ pressure of 6.7 Pa and the RF power of 50 W in a sputtering chamber (Fig. 2(c)). This plasma treatment is very important since the surface layer of the base electrodes may be contaminated and/or have other nonsuperconducting phases.[7] The counter electrodes were then deposited by sputtering. Device processing was completed by lithographic patterning (Fig. 2(d)).

Figure 3 shows resistance versus temperature characteristics for the base and counter electrodes. The temperature dependence of the dc resistance of the films was measured by the conventional four-probe method with dc current. The normal-state dependence is approximately linear and decreases with temperature. The normal state to superconducting transition for this junction is
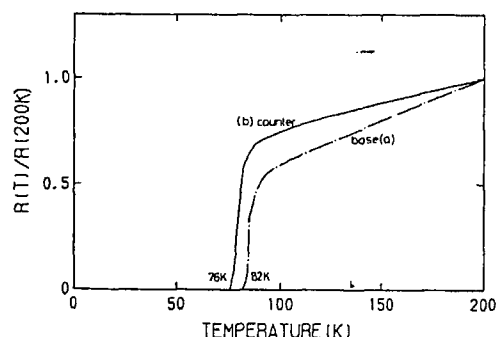
Fig. 3. Resistance vs temperature for (a) base electrode and (b) counter electrode.
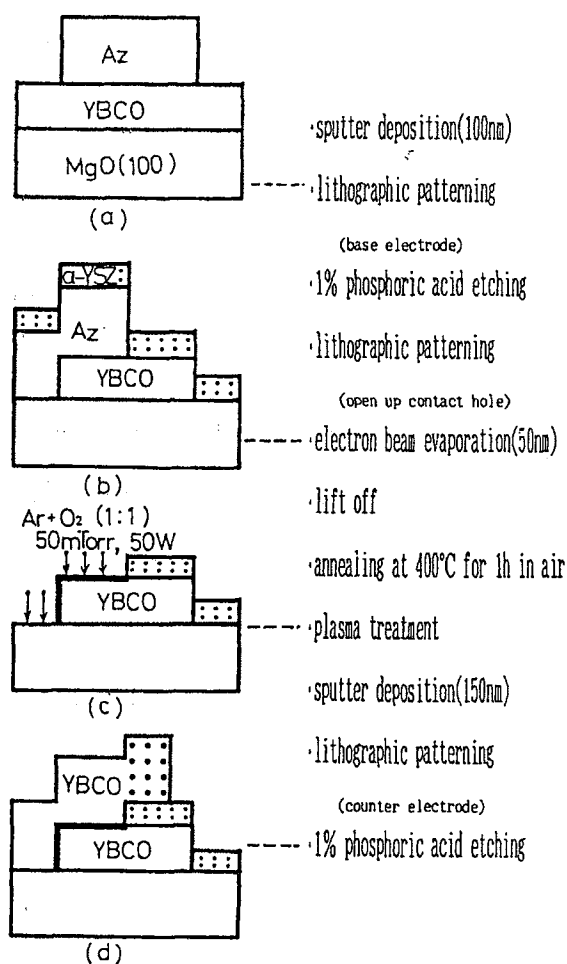
Fig. 2. Fabrication process of a all-high-T_c Josephson junction.

(a)
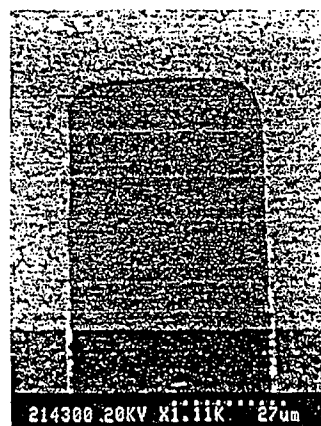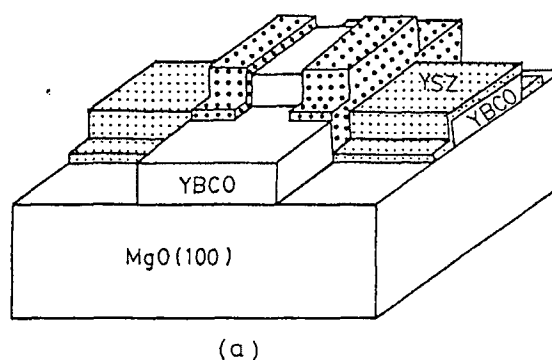
(b) SEM   49×52μm²

Fig. 4. Schematic diagram of (a) the junction geometry; SEM miorograph of (b) a finished junction.

very sharp. The T_c for the base and counter electrodes was 82 K and 76 K, respectively.

Figure 4(a) shows a schematic figure of a junction fabricated on the MgO(100) substrate. Both the electrodes of the base and the counter electrodes are grown epitaxially on the same substrate with their c-axes normal to the substrate. A scanning electron microscopy (SEM) picture of a junction is shown in Fig. 4(b). The junction
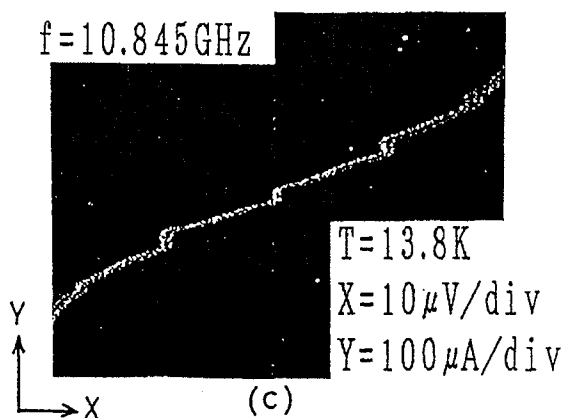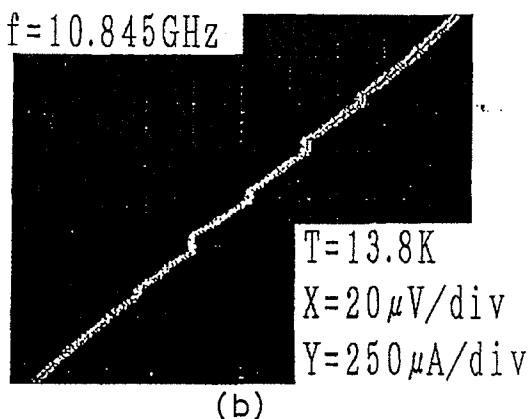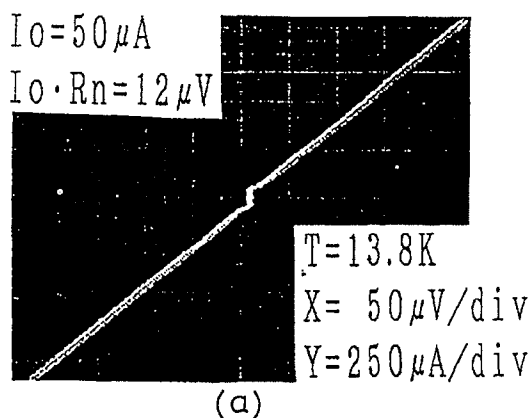
Fig. 6.   Critical current vs temperature of the YBCO/barrier/YBCO junction.

has no grain boundary.

Figure 5(a) shows the current-voltage (I-V) characteristics of a YBCO/barrier/YBCO junction. The junction shows S/N/S or S/S'/S-type characteristics. Under the irradiation of 10.845 GHz wave, clear Shapiro steps appeared in the I-V characteristic at the voltages $V_n = nhf/2e$ (Figs. 5(b)–5(c)). Moreover, the height of the first step oscillates according to the increase of irradiation power. The critical current of this junction was modulated by the ambient magnetic field. The $I_c - R_n$ product was determined to be 12 μV.

Figure 6 shows the critical current I_c, measured using a 10 μV detection, as a function of temperature. At 76 K, the critical current was observed. In this study, the critical current and the transition temperatures of the base and counter electrodes were lower than thin films obtained by lithographical patterning and the chemical etching technique.

In conclusion, all-high-T_c Josephson junctions consisting of a YBCO/barrier/YBCO-layered structure using epitaxial YBCO films sputtered on MgO(100) have been successfully fabricated. The barrier layer was obtained by Ar + O$_2$ plasma treatment of the surface of the base electrodes without a grain boundary or insulating films. These junctions show superconductor/normal-metal/superconductor (SNS)-like current-voltage characteristics. Constant-voltage current steps observed in response to 10 GHz microwave radiation show that ac-Josephson effects occur in these junctions.

Fig. 5.   The typical current-voltage (I-V) characteristics for all-high-T_c junction is shown in (a), (b)–(c) show I-V characteristics for the junction exposed to f = 10.845 GHz microwave.

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USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT B.2

United States Patent [19]

Chan

[54] **HIGH-TEMPERATURE SSNS AND SNS JOSEPHSON JUNCTION AND METHOD OF MAKING JUNCTION**

[75] Inventor: **Hugo W. Chan**, Palos Verdes Estates, Calif.

[73] Assignee: **TRW Inc.**, Redondo Beach, Calif.

[21] Appl. No.: **761,412**

[22] Filed: **Dec. 6, 1996**

[51] Int. Cl.^{6} **H01L 29/06**

[52] U.S. Cl. **257/31**; 257/33; 257/35; 505/190

[58] Field of Search 257/30, 31, 32, 257/33, 34, 35, 36, 37, 38, 39; 505/190

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Strikovskiy, M.D. et al., "Ramp–type YBa$_2$Cu$_3$O$_{7-\delta}$ Josephson junctions with high characteristic voltage, fabricated by a new, completely in situ, growth technique," *Appl. Phys. Lett.* 69(19):2918–2920 (1996).

Primary Examiner—Sara Crane
Attorney, Agent, or Firm—Michael S. Yatsko

[57] **ABSTRACT**

A high temperature superconductor junction and a method of forming the junction are disclosed. The junction **40** comprises a first high-T$_c$, superconductive layer (first base electrode layer) **46** on a substrate **42** and a dielectric layer **48** on the first high-T$_c$, superconductive layer. The dielectric layer and the first high-T$_c$ superconductive layer define a ramp edge **50**. A trilayer SNS structure **52** is disposed on the ramp edge to form an SSNS junction. The SNS structure comprises a second high-T$_c$, superconductive layer (second base electrode layer) **54** directly on the first high-T$_c$ superconductive layer, a normal barrier layer **56** on the second high-T$_c$ superconductive layer, and a third high-T$_c$ superconductive layer **58** (counterelectrode) on the barrier layer. The ramp edge is typically formed by photoresist masking and ionmilling. A plasma etch step can be performed in-situ to remove the photoresist layer **62** following formation of the ramp edge. A normal-superconductive (NS) structure can be optimally formed directly on the ramp edge following the plasma etch step to form an SNS junction **70**. The SNS and NS structures are preferably formed in-situ.
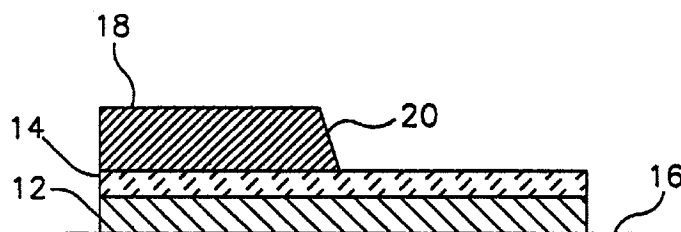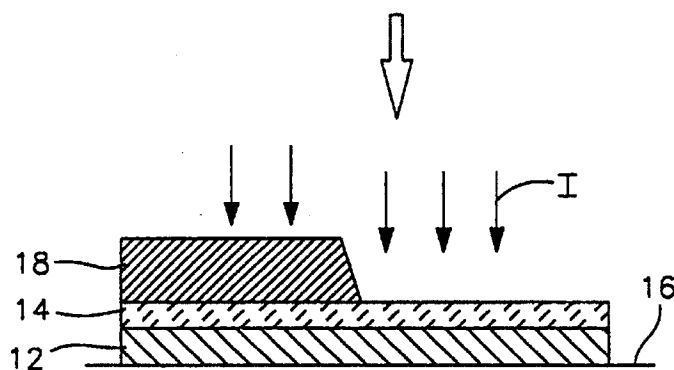
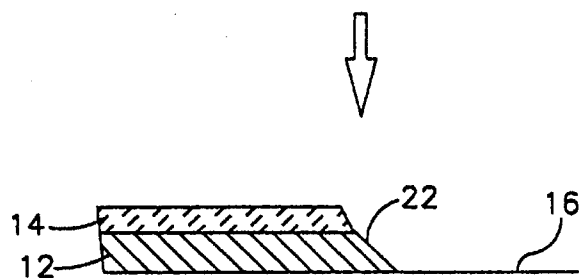**9 Claims, 6 Drawing Sheets**
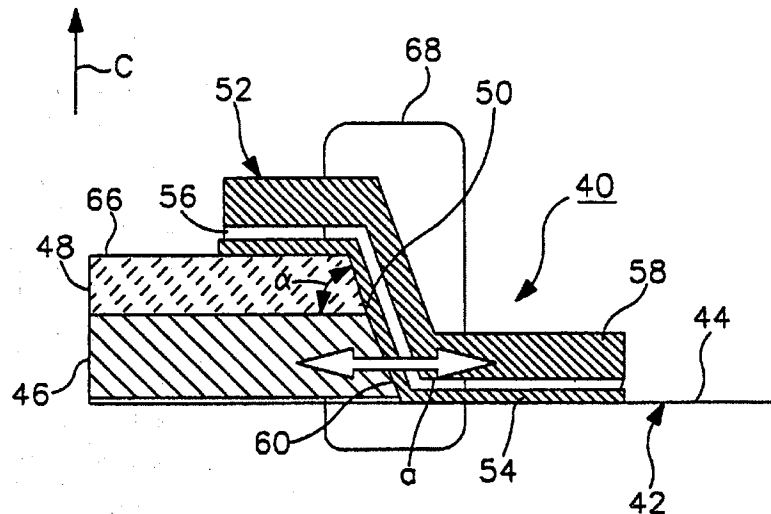
FIG. IA

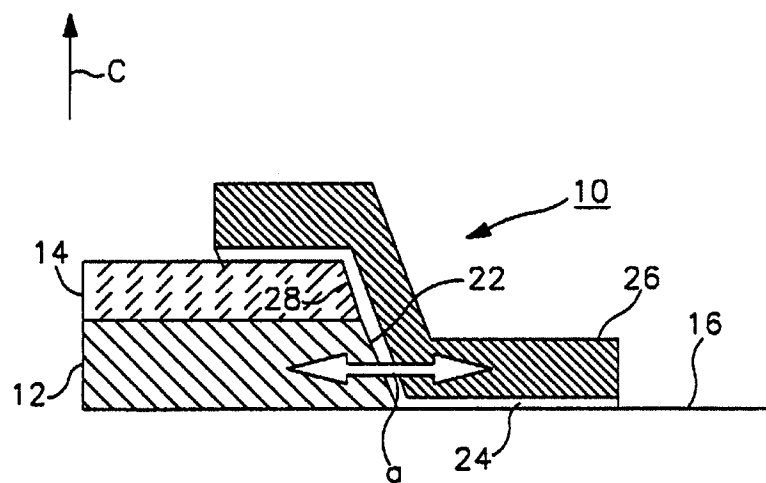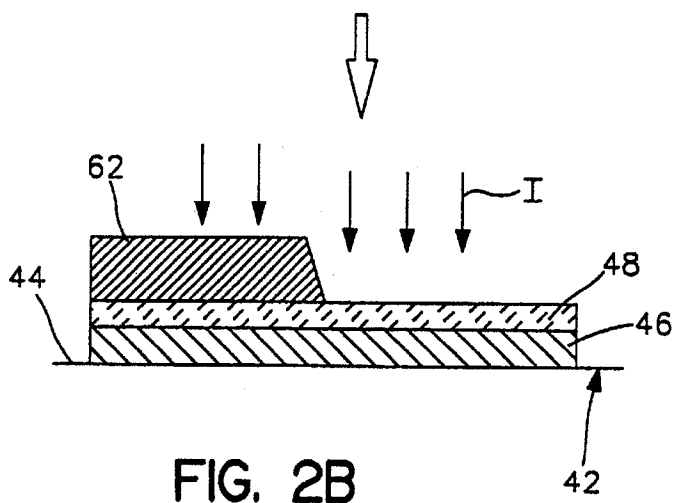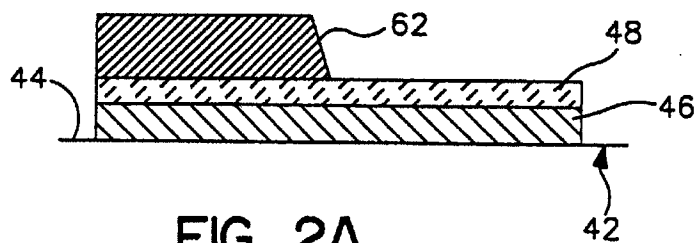PRIOR ART

FIG. IB

PRIOR ART

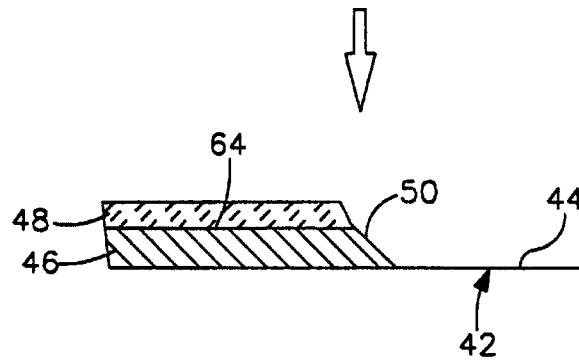FIG. IC

FIG. ID

FIG. 2A

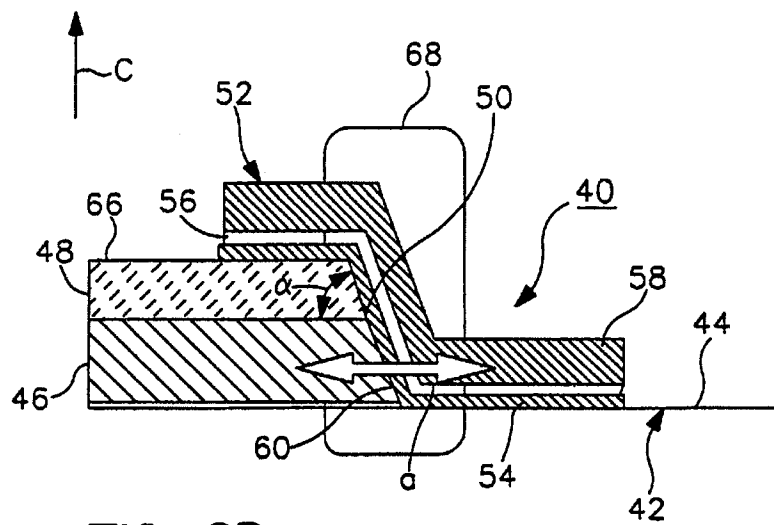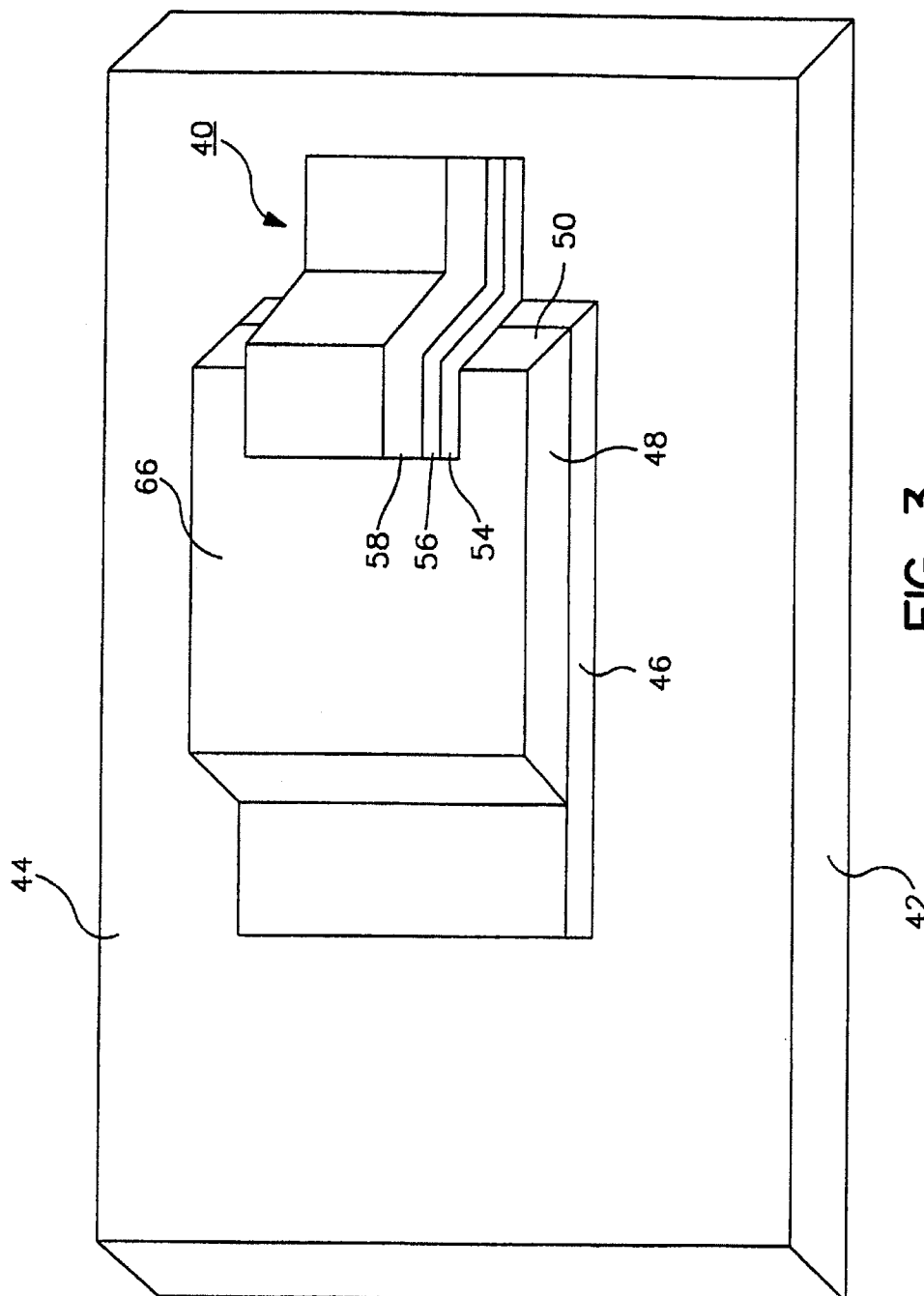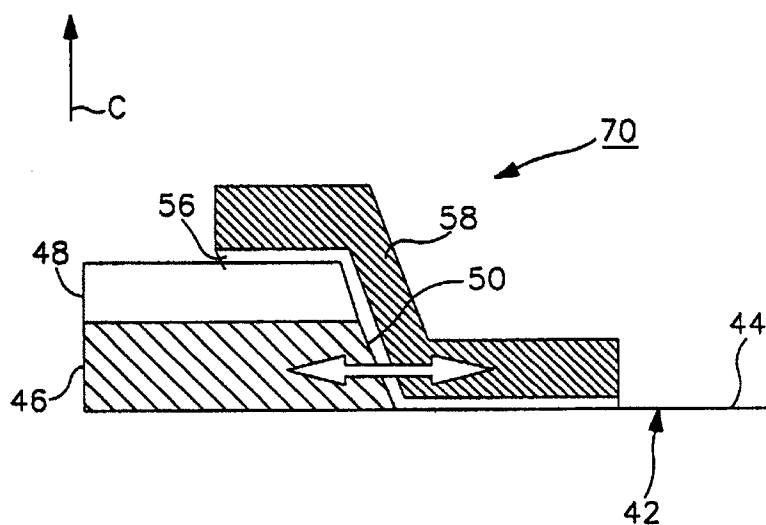FIG. 2B

FIG. 2C

FIG. 2D

FIG. 3

FIG. 4

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HIGH-TEMPERATURE SSNS AND SNS JOSEPHSON JUNCTION AND METHOD OF MAKING JUNCTION

BACKGROUND

The invention is directed to the field of superconducting Josephson junctions and, more particularly, to a high-temperature superconductive—superconductive-normal-superconductive (SSNS) Josephson junction and a high-temperature superconductive-normal-superconductive (SNS) Josephson junction and a method of making the junctions.

High-temperature superconductive (HTS) materials have a normal-to-superconducting transition temperature, T_c, of more than 25 K. At lower temperatures, these materials exhibit no resistance to electrical current flow. High-T_c superconductive materials are used in HTS circuits. In comparison to low-temperature superconductive (LTS) circuits, HTS circuits operate at significantly higher temperatures, typically about 25–100 K as compared to about 4–10 K for LTS circuits. HTS circuits are highly advantageous as compared to LTS circuits due to their relatively reduced cooling and insulation requirements.

HTS circuits can be used in a wide range of defense, industrial and commercial applications. HTS circuits can be used in analog-to-digital (ADC) applications such as analog signal processors (ASP), digital signal processors (DSP), high-speed computers, asynchronous transfer mode (ATM), switching networks, telecommunications, commercial satellites; rf applications such as resonators, band-pass filters, phased-array antennae for cellular/satellite telecommunications; and sensors such as magnetic sensors for mine-detection, anti-submarine warfare, and bio-magnetic diagnostic and non-destructive magnetic sensors.

HTS circuits are a vital next generation technology capable of replacing existing semiconductor technologies and having a tremendous growth potential within the next decade.

Despite providing important advantages, known HTS circuits have performance limiting problems as well. One basic problem of HTS circuits is the non-uniformity of the active devices. The basic active device used in HTS circuits is the Josephson junction. A key junction technology is the SNS Josephson junction. SNS Josephson junctions include two superconductive layers and an intermediate barrier layer (N layer) comprised of a normal material. During operation, a supercurrent flows through the barrier layer via the Josephson tunneling effect.

In known ramped high-T_c SNS Josephson junctions, the SNS junction is formed by depositing the normal barrier layer and a high-T_c superconductive counterelectrode layer on a ramped high-T_c superconductive base electrode. One of the performance-limiting problems associated with known ramped SNS junctions is the occurrence of interfacial electric resistance at the base electrode/normal barrier layer interface at the ramp edge. This interfacial resistance is the result of the conventional fabrication process used to form the junction. Particularly, the base electrode is exposed to ambient conditions and to chemical treatments during the patterning process. As a result, the top several monolayers of the base electrode are degraded and deoxygenated, reducing the quality of these monolayers as compared to the bulk of the layer, and producing a resistive and/or nonuniform interface.

A resistive and/or non-uniform junction interface adversely affects process quality control by increasing the non-uniformity of the junction characteristics.

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A technique that has been used in an attempt to overcome the problem of interfacial resistance in SNS junctions is low-energy ion-etch cleaning of the interface surface, either ex-situ before depositing the normal barrier layer and the counterelectrode layer, or, alternately, in-situ in the same vacuum system in which the barrier layer and counterelectrode layer are deposited. Ion-etch cleaning invariably also produces lattice damage in the exposed ramp edge of the base electrode, adversely affecting the interfacial electrical properties. Thus, this technique has not overcome the problem of interfacial resistance between the base electrode and the normal barrier layer in known SNS junctions.

A known technique of fabricating high-V_c SNS Josephson junctions in-situ employs shadow masking. Particularly, a shadow mask is patterned on the substrate, and the base electrode is deposited by orienting a source at an angle relative to the shadow mask to form the ramp edge. The substrate is then rotated, and the barrier layer and the counterelectrode layer are deposited with the source oriented at a vertical angle relative to the substrate. The shadow mask is then removed.

This technique has proven less than satisfactory because the steps for forming the ramp edge are directional dependent and, so, junctions cannot be fabricated in an arbitrary direction of the substrate. This factor is a major limitation in integrated circuit process technology. In addition, the substrate cannot be rotated during the deposition process; consequently, the thickness of each of the deposited layers can vary significantly across the substrate. This non-uniformity is particularly severe in off-axis sputtering techniques which form a thickness gradient across the substrate unless the substrate is rotated, or unless special techniques are employed to randomize material deposition across the substrate.

Thus, there is a need for an improved high-T_c Josephson junction that (i) overcomes the problem of electrical resistance at the base electrode/normal barrier layer interface and preserves the quality of the interfaces between the normal barrier layer and the adjacent superconductive layers; (ii) provides enhanced junction I_c, and enhanced junction V_c uniformity; and (iii) can be formed by a non-directional dependent process.

SUMMARY

The present invention satisfies the above needs. The present invention provides an improved high-T_c, superconductive—superconductive-normal-superconductive (SSNS) Josephson junction and a method of making the SSNS junction. The present invention also provides an improved high-T_c superconductive-normal-superconductive (SNS) junction and a method of making the SNS junction. More specifically, the high-T_c, SSNS and SNS Josephson junctions (i) eliminate the problem of electrical resistance at the base electrode/normal barrier layer interface and preserves the quality of the interfaces between the normal barrier layer and the adjacent superconductive layers; (ii) provide enhanced junction I_c, and enhanced V_c uniformity; (iii) provide reduced parasitic junction leakage current; and (iv) are formed by a nondirectional dependent process.

The high-T_c SSNS Josephson junction according to the present invention is formed on a suitable substrate typically comprised of a dielectric material. The junction comprises a first high-T_c, superconductive (HTS) layer on the substrate, and a dielectric layer on the first HTS layer. The first HTS layer and the dielectric layer define a ramp edge.

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A trilayer SNS structure is disposed on the ramp edge to form a four-layer SSNS junction. The trilayer SNS structure comprises a second high-T_c superconductive (HTS) layer directly on the ramp edge, a barrier layer of a normal material (i.e., a material that is non-superconductive at the operating temperature of the junction) on the second HTS layer, and a third high-T_c superconductive (HTS) layer on the barrier layer. The first and second HTS layers form a two-layer base electrode. The second HTS layer is thinner than the first HTS layer. The third HTS layer functions as the counterelectrode in the SSNS Josephson junction.

The first, second and third HTS layers are typically comprised of the same high-T_c superconductive material.

According to the present invention, the method of forming the high-T_c SSNS Josephson junction comprises depositing the first HTS layer on the substrate; depositing the dielectric layer on the first HTS layer; and forming the ramp edge on the first HTS layer and the dielectric layer.

Next, the trilayer SNS structure is formed on the ramp edge by sequentially depositing the second HTS layer on the ramp edge; the barrier layer on the second HTS layer; and the third HTS layer on the barrier layer.

The ramp edge is formed using a conventional photoresist masking technique. To prevent contamination of the ramp edge prior to formation of the SNS structure, the photoresist layer disposed on the dielectric layer is preferably removed in-situ using a dry plasma etch process. The plasma is generated from an oxygen-containing gas which also replenishes depleted oxygen in the first HTS layer at the ramp edge.

A normal-superconductive (NS) structure or preferably the above-described SNS structure can be formed on the ramp edge following the plasma etch step. The respective resulting SNS and SSNS junctions each have improved electrical properties as compared to known SNS junctions.

The SNS and NS structures are preferably formed in-situ on the ramp edge to minimize contamination.

An optional implant step can be performed to delineate the SSNS or SNS junction region. This step can be performed before of after the SNS (or NS) structure is formed on the ramp edge.

DRAWINGS

These and other features, aspects and advantages of the present invention will become better understood from the following description, appended claims and accompanying drawings, where:

FIGS. 1a–1d are an illustrational flow chart of the steps of forming an SNS Josephson junction according to a known process; and

FIGS. 2a–2d are an illustrational flow chart of the steps of forming an improved SSNS Josephson junction according to the present invention;

FIG. 3, is a perspective view of the SSNS junction of FIG. 2d; and

FIG. 4 illustrates an improved SNS Josephson junction according to another embodiment of the present invention.

DESCRIPTION

The present invention is directed to a high-temperature superconducting junction having improved quality and performance characteristics and a method of forming the junction. The superconducting junction can be a superconductive—superconductive-normal-

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superconductive (SSNS) junction 40 as shown in FIGS. 2d and 3, or a superconductive-normal-superconductive (SNS) junction 70 as shown in FIG. 4.

FIGS. 1a–1d illustrate sequential steps of a known process for forming a known SNS junction structure 10. The process comprises depositing a first high-T_c superconductive (HTS) layer (base electrode layer) 12 and a dielectric layer 14 on a substrate 16. As used herein, the term "T_c" is the critical temperature below which superconductive materials exhibit zero electrical resistivity, and "high-T_c, superconductive materials" are materials that are superconductive above about 25 K. A photoresist layer 18 is formed on the dielectric layer 14 and the photoresist layer 18 is then patterned to form an inclined surface 20. As depicted in FIG. 1b by arrows I, ion mill etching is then performed to remove a portion of the dielectric layer 14 and the first HTS layer 12 to define an inclined ramp edge 22 as shown in FIG. 1c.

The photoresist layer 18 is then stripped from the dielectric layer 14, typically using a wet chemical stripping process. The ex-situ wet stripping process can contaminate and deoxygenate the ramp edge 22. Superconductive materials such as yttrium-barium-copper oxide (YBCO) are very reactive and exposed surfaces of thin films of these materials are easily contaminated by contact with air during photolithographic processing and, as a result, not able to support the growth of overlying deposited layers with the preferred crystal structure. In addition, the superconducting properties of the contaminated films can be degraded.

To remove contamination, the ramp edge 22 can be cleaned using a low-energy ion cleaning process to form the first HTS layer 12 and the dielectric layer 14.

Next, a barrier layer 24 comprised of a normal material and a second high-T_c, superconductive (HTS) layer 26 (counterelectrode layer) are sequentially deposited on the ramp edge 22. As used herein, "normal materials" are materials that are non-superconductive at the temperature of operation of the Josephson junction.

Finally, the SNS structure is patterned and defined using a conventional photoresist masking technique followed by ion-mill etching to form the SNS junction 10 shown in FIG. 1d. The c-axis direction is indicated by the arrow c. In the SNS junction 10, the current flow path is to/from the first HTS layer 12 laterally in the direction of the a-axis (represented by arrow a in FIG. 1d) across the first HTS layer 12, and the barrier layer 24 to/from the second HTS layer 26.

The low-energy ion cleaning of the ramp edge 22 removes the top few contaminated monolayers of the first HTS layer 12, but also produces undesirable lattice damage in the ramp edge 22. Consequently, the structure and quality of the interface 28 between the first HTS layer 12 and the barrier layer 24 are degraded. The interface 28 is resistive and/or non-uniform, which adversely impacted the uniformity of the characteristic voltage V_c of the junction 10. $V_c = I_c R_n$, where I_c is the critical Josephson junction current, the maximum supercurrent that the junction can sustain, and R_n is the electrical resistivity of the Josephson junction. As a result, large scale HTS integrated circuits integrating the junction 10 cannot be fabricated.

The present invention overcomes the problem of interfacial resistance associated with the known SNS Josephson junction 10 and provides a superconducting junction having improved operational performance.

FIGS. 2d and 3 illustrate a superconductive—superconductive-normal-superconductive (SSNS) Josephson junction 40 according to the present invention. The

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junction 40 is formed on a substrate 42 having a planar upper surface 44. The junction 40 comprises a first high-T_c superconductive (HTS) layer 46 (first base electrode layer) comprised of a high-T_c superconductive material provided on the upper surface 44 of the substrate 42, and a dielectric layer 48 disposed on the first HTS layer 46. The dielectric layer 48 is comprised of a suitable dielectric material to provide electric insulation between the first HTS layer 46 and overlying layers as described below.

The first HTS layer 46 and the dielectric layer 48 define an inclined face referred to herein as the ramp edge 50.

A trilayer SNS structure 52 is disposed on the ramp edge 50. The trilayer SNS structure 52 comprises a second high-T_c superconductive (HTS) layer 54 (second base electrode layer) of a high-T_c superconductive material directly on the ramp edge 50, a barrier layer 56 of a normal material on the second HTS layer 54, and a third high-T_c superconductive (HTS) layer 58 (counterelectrode layer) comprised of a high-T_c superconductive material on the barrier layer 56.

In the SSNS junction 40, the first HTS layer 46, second HTS layer 54 and third HTS layer 58 are preferably epitaxial with a c-axis substantially normal to the upper surface 44 of the substrate 42 as represented by arrow c in FIG. 2d. The dielectric layer 48 and the barrier layer 56 are typically also epitaxial with a c-axis in substantially the same direction as the superconductive layers.

In the SSNS Josephson junction 40, the ramp edge 50 does not directly contact the barrier layer 56. Rather, the ramp edge 50 advantageously directly contacts the second HTS layer 54. As a result, the junction 40 eliminates the problem of electric resistance and non-uniformity at the interface 28 between the first HTS layer 12 and the barrier layer 24 in the known SNS junction 10.

In addition, the present invention overcomes the problems associated with known directional dependent processes.

The high-T_c SSNS Josephson junction 40 provides strong phase coupling of the superconductive Cooper electron pairs between the first HTS layer 46 and the second HTS layer 54, and significantly reduces any detrimental effects caused by the presence of contamination at the interface 60 at the ramp edge 50. The trilayer SNS structure 52 preserves the quality of the interface between the second HTS layer 54 and the barrier layer 56 and the interface between the barrier layer 56 and the third HTS layer 58. The resulting SSNS Josephson junction 40 provides low interfacial electric resistance between the first HTS layer 46 and the second HTS layer 54, and enhanced I_cR_n, uniformity.

A method of forming the high-T_c SSNS Josephson junction 40 according to the present invention is depicted in FIGS. 2a–2d. The SSNS Josephson junction 40 is formed on the upper surface 44 of the substrate 42. The substrate 42 is typically comprised of a dielectric material that, has lattice parameters closely matching that of the crystallographic face of the first HTS layer 46 perpendicular to the c-axis; i.e., the face in the a-axis direction. The substrate 42 is typically a single crystal material. An excellent material for the substrate 42 is lanthanum aluminate ($LaAlO_3$) which promotes c-axis epitaxial growth of $YBa_2Cu_3O_{7-x}$ (YBCO). Other suitable substrate 42 materials that promote c-axis epitaxial growth of YBCO can also be used, including $SrTiO_3$ (strontium titanate), neodymium gallate, strontium aluminum tantalate and the like. For high-T_c superconductive materials other than YBCO forming the first HTS layer 46, the substrate 42 can be comprised of $LaAlO_3$ and other suitable materials that promote c-axis epitaxial growth of the first HTS layer 46.

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The first HTS layer 46 (first base electrode layer) is comprised of a high-T_c superconductive material deposited as a thin film on the upper surface 44 of the substrate 42. The first HTS layer 46 is typically comprised of a high-T_c superconductive material selected from the YBCO system ($YBa_2Cu_3O_{7-x}$, where x is typically a low value of about 0.1). These materials have a critical temperature, T_c, of about 85 K to about 92 K when deposited as a thin film. Other suitable high-$_c$ superconductive materials can be used to form the first HTS layer 46. Such other materials include, for example, compounds of the system $A_2B_2Ca_nCu_{n+1}O_{2n+6}$, where n=0, 1, 2, 3 or 4, A=Bi or Tl, and B=Sr or Ba; and compounds of the system $LnBa_2Cu_3O_{7-x}$, where Ln=Nd, Sm, Er, Gd, Dy, Ho, Er, Tm or Lu.

The first HTS layer 46 is epitaxially grown on the substrate 42 in the c-axis direction represented by arrow c, using a conventional thin film deposition process. Preferably, a physical vapor deposition (PVD) process is used to restrict contamination levels. Suitable PVD processes include, for example, laser ablation, sputtering and the like.

The first HTS layer 46 typically has a thickness of from about 1000 Å to about 4000 Å.

Next, the dielectric layer 48 is deposited on the first HTS layer 46 in-situ in the same deposition system. The dielectric layer 48 is typically epitaxially grown in the c-axis direction using a suitable thin film deposition process such as, laser ablation, sputtering and the like. The dielectric layer 48 is comprised of a suitable dielectric material such as $SrTiO_3$, $LaAlO_3$, neodymium gallate, strontium aluminum tantalate and the like.

The dielectric layer 48 typically has a thickness of from about 500 Å to about 3000 Å.

Next, a photoresist layer 62 is deposited on the dielectric layer 48. The photoresist layer 62 is comprised of a conventional material and is patterned using a conventional photoresist masking technique to enable the subsequent formation of the ramp edge 50 shown in FIGS. 2c and 2d.

The ramp edge 50 is typically formed by a conventional ion mill etching process. As shown in FIG. 2d, the ramp edge 50 is inclined upwardly at an angle α relative to the planar upper surface 44 of the substrate 42. This angle is typically from about 5° to about 90°, and preferably from about 5° to about 30°.

The photoresist layer 62 can be removed using a conventional wet stripping process performed at ambient conditions. This step can, however, contaminate the ramp edge 50 surface.

According to the present invention, the photoresist layer 62 is preferably stripped in the same vacuum system and not exposed to room ambient conditions and wet etching chemicals. Particularly, instead of breaking vacuum and removing the as formed structure for wet etching, the structure is maintained within the vacuum system and the photoresist layer 62 is stripped in-situ by contact with a plasma generated from an oxygen containing gas such as O_2. Consequently, potential contamination of the ramp edge 50 surface is minimized.

In addition, the plasma dry etch process can reoxidize oxygen-depleted regions of the high-T_c superconductive material forming the first HTS layer 46 to ensure a high-T_c value is maintained.

The plasma etch step is preferably performed in the system used to subsequently form the trilayer SSNS structure 52. For example, the plasma etch of the photoresist layer

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62 can be performed in a common vacuum chamber, or preferably in a dedicated vacuum chamber used for photoresist stripping, located within a multi-chamber, multi-function cluster tool system.

A suitable cluster tool system for performing these steps is the cluster tool system manufactured by DCA Inc. Other companies that manufacture cluster tool systems included Applied Material, LAM Research, Leskers and the like.

The plasma etch removal of the photoresist layer 62 produces minimal chemical damage to the ramp edge 50. As represented by arrows I in FIG. 2b, low-energy ion cleaning can be used to clean the ramp edge 50 to remove any such minimal contamination before forming the trilayer SNS structure 52.

After the ramp edge 50 is cleaned following plasma etching, the barrier layer 56 and the third HTS layer 58 can be sequentially deposited on the ramp edge 50 to produce an SNS junction 70 shown in FIG. 4. The SNS junction 70 has reduced interfacial resistance and increased uniformity between the first HTS layer 46 and the overlying barrier layer 56 as compared to the known SNS junction 10 shown in FIG. 1d.

Preferably, the trilayer SNS structure 52 is formed on the ramp edge 50 to produce the SSNS junction 40. The trilayer SNS structure 52 comprises the second HTS layer 54 (second base electrode layer) disposed directly on the ramp edge 50, the barrier layer 56 on the second HTS layer 54, and the third HTS layer 58 (counterelectrode layer) on the barrier layer 56. By forming the trilayer SNS structure 52 on the ramp edge 50, the advantages of using plasma etching to remove the photoresist layer 62 and the advantages provided by the trilayer SNS structure 52 are realized in the resulting SSNS junction 40.

The trilayer SNS structure 52 is preferably formed in-situ in the same system used to form the structure illustrated in FIG. 2c without breaking the vacuum; i.e., the same vacuum system, or alternately, a dedicated vacuum chamber for SNS film deposition within the same multi-chamber cluster tool system.

The second HTS layer 54 is deposited so that it overlies the ramp edge 50, the upper surface 44 of the substrate 42, and a portion of the upper surface 66 of the dielectric layer 48. The second HTS layer 54 is preferably comprised of the same high-T_c superconducting material as the first HTS layer 46 to provide matched lattice parameters, coefficients of thermal expansion and electrical properties, as well as chemical compatibility.

The second HTS layer 54 typically has a thickness of from about 100 Å to about 1000 Å, and preferably has a thickness of less than about 500 Å. It is advantageous to maintain the second HTS layer 54 at a thickness of less than about 500 Å so that the cross-sectional area of the second HTS layer 54 is maintained small also. If this cross-sectional area is too large, the portions of the second HTS layer 54, the barrier layer 56 and the third HTS layer 58 overlying the upper surface 66 of the dielectric layer 48 can function as part of the junction and effectively increase the junction geometry.

The second HTS layer 54 is preferably epitaxially grown in the c-axis direction using a suitable thin film deposition technique such as used to form the first HTS layer 46.

Next, preferably without breaking vacuum in the deposition system, the barrier layer 56 is deposited on the second HTS layer 54. The barrier layer 56 is comprised of a normal material that is non-superconductive at the temperature of operation of the SSNS junction 40. Suitable materials include cobalt-doped YBCO, cobalt-doped praseodymium

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barium copper oxide (cobalt-doped PBCO), gallium-doped PBCO and the like.

The barrier layer 56 typically has a thickness of from about 50 Å to about 1000 Å. The barrier layer 56 is typically also epitaxially grown in the c-axis direction on the second HTS layer 54 using a suitable thin film deposition technique.

Next, preferably without breaking vacuum, the third HTS layer 58 is deposited on the barrier layer 56. The third HTS layer 58 is typically formed of the same high-T_c superconductive material used to form the second HTS layer 54 and the first HTS layer 46.

The third HTS layer 58 typically has a thickness of from about 500 Å to about 5000 Å and is typically also epitaxially grown in the c-axis direction using a suitable thin film deposition technique. The third HTS layer 58 can be deposited using the same thin film deposition technique used to form the first HTS layer 46 and the second HTS layer 54.

Following deposition of the second HTS layer 54, the barrier layer 56 and the third HTS layer 58, the trilayer SNS structure 52 is typically patterned and defined using a conventional photoresist masking technique followed by ion-mill etching, to produce the SSNS Josephson junction 40 as shown in FIG. 2d.

According to the present invention, an optional implant maskstep can be performed after the trilayer SNS structure 52 is formed as depicted at 68 in FIG. 2d. The implant step delineates the junction region by implanting a suitable species such as silicon ions effective to destroy the superconductive characteristics of the second HTS layer 54 away from the trilayer SNS structure 52. A conventional ion implantation technique can be used to implant the species.

In the SSNS Josephson junction 40, the current flow path is from/to the first HTS layer 46 laterally (in the a-axis direction) across the second HTS layer 54, and the barrier layer 56 laterally to/from the third HTS layer 58, as depicted by the arrow a in FIG. 2d. The thinness of the second HTS layer 54 minimizes parasitic junction leakage current. Reduced phase coupling of superconducting current Cooper pairs in the c-axis direction significantly reduces the parasitic junction leakage current.

As compared to the known SNS junction 10 shown in FIG. 1d, the present SSNS Josephson junction 40 has reduced base electrode layer (second HTS layer 54) to barrier layer 56 interface electrical resistance, enhanced I_c, and enhanced V_c uniformity.

As an example, an SSNS junction 40 including a first HTS layer 46, a second HTS layer 54 and a third HTS layer 58 comprised of YBCO, an upper layer comprised of strontium titanate, a normal barrier layer 56 comprised of cobalt-doped YBCO, and having a width of about 4 microns typically has a I_c value of from about 100 microamps to about 500 microamps, and a V_c value of from about 100 microvolts to about 400 microvolts.

The present invention can be used in HTS integrated circuits having enhanced gate complexity. The high V_c of the present invention enables larger signal values for improved output driving capability and improved immunity against background noise, and also high speed of operation.

Furthermore, the base electrode formed of the first HTS layer 46 and the second HTS layer 54, and the counterelectrode (third HTS) layer 58 can be used as separate interconnect layers, allowing one layer to cross over the other layer.

Although the present invention has been described in considerable detail with reference to certain preferred versions thereof, other versions are possible. Therefore, the

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scope of the appended claims should not be limited to the description of the preferred versions contained herein.

What is claimed is:

1. A high-T_c superconducting Josephson junction, comprising:

a) a substrate having a surface;

b) a first high-T_c superconductive layer on the surface of the substrate, the first high-T_c superconductive layer having a first thickness;

c) a dielectric layer on the first high-T_c superconductive layer;

d) a ramp edge on the first high-T_c layer and the dielectric layer, the ramp edge being inclined in a nondirectional dependent disposition relative to the surface of the substrate;

e) a second high-T_c superconductive layer on the ramp edge, the second high-T_c superconductive layer having a second thickness less than the first thickness;

f) a barrier layer on the second high-T_c superconductive layer, the barrier layer being comprised of a normal material that is non-superconductive at the operating temperature of the superconducting junction; and

g) a third high-T_c superconductive layer on the barrier layer, wherein

each of said first, second and third high-T_c superconductors are of uniform thickness.

2. The superconducting junction of claim **1**, wherein the first high-T_c superconductive layer, the second high-T_c superconductive layer and the third high-T_c superconductive layer are comprised of the same high-T_c superconductive material.

3. The superconducting junction of claim **2**, wherein the high-T_c superconductive material is a material selected from the group consisting of YBCO; $A_2B_2Ca_nCu_{n+1}O_{2n+6}$, where n=0, 1, 2, 3 or 4, A=Bi or Tl, and B=Sr or Ba; and $LnBa_2Cu_3O_{7-x}$, where Ln=Nd, Sm, Er, Gd, Dy, Ho, Er, Tm or Lu.

4. The superconducting junction of claim **3**, wherein the dielectric layer is comprised of a material selected from the group consisting of $SrTiO_3$, $LaAlO_3$, neodymium gallate and strontium aluminum tantalate, and the barrier layer is comprised of a material selected from the group consisting of cobalt-doped YBCO, cobalt-doped PBCO and gallium-doped PBCO.

5. The superconducting junction of claim **1**, wherein the second high-T_c superconductive layer has a thickness of from about 100 Å to about 1000 Å.

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6. The superconducting junction of claim **5**, wherein the second high-T_c superconductive layer has a thickness of less than about 500 Å.

7. The superconducting junction of claim **1**, wherein the ramp edge is oriented at an angle of from about 5° to about 30° relative to the surface of the substrate.

8. The superconducting junction of claim **1**, wherein the first high-T_c superconductive layer, the second high-T_c superconductive layer, the barrier layer and the third high-T_c superconductive layer are epitaxial with a c-axis in a direction substantially normal to the surface of the substrate.

9. A high-T_c superconducting Josephson junction, comprising:

a) a substrate having a surface;

b) a first high-T_c superconductive layer on the surface of the substrate, the first high-T_c superconductive layer having a first thickness;

c) a dielectric layer on the first high-T_c superconductive layer;

d) a ramp edge on the first high-T_c superconductive layer and the dielectric layer, the ramp edge being inclined in nondirectional dependent disposition relative to the surface of the substrate;

e) a second high-T_c superconductive layer on the ramp edge, the second high-T_c superconductive layer having a second thickness less than the first thickness;

f) a barrier layer on the second high-T_c superconductive layer, the barrier layer being comprised of a normal material that is non-superconductive at the operating temperature of the superconducting junction; and

g) a third high-T_c superconductive layer comprised of a high-T_c superconductive material on the barrier layer;

h) wherein i) the first high-T_c superconductive layer, the second high-T_c superconductive layer, the barrier layer and the third high-T_c superconductive layer are epitaxial with a c-axis substantially normal to the surface of the substrate, ii) the first high-T_c superconductive layer, the second high-T_c superconductive layer and the third high-T_c superconductive layer are comprised of the same high-T_c superconductive material, and iii) the second high-T_c superconductive layer has a thickness of less than about 500 Å.

*   *   *   *   *

USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT B.3

HIGH TEMPERATURE SUPERCONDUCTOR JOSEPHSON WEAK LINKS

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High T_c edge-geometry SNS microbridges have been fabricated using ion-damaged $YBa_2Cu_3O_{7-x}$ (YBCO) and a nonsuperconducting phase of YBCO (N-YBCO) as normal metals. Optimization of the ion milling process used for YBCO edge formation and cleaning has resulted in ion-damage barrier devices which exhibit I-V characteristics consistent with the Resistively-Shunted-Junction (RSJ) model, with typical current densities (J_c) of $\approx 5 \times 10^6$ A/cm^2 at 4.2 K. Characterization of N-YBCO films suggests that N-YBCO is the orthorhombic YBCO phase with oxygen disorder suppressing T_c. Weak links using N-YBCO as the normal metal show RSJ I-V characteristics and exponential scaling of J_c, with a normal metal coherence length of ≈ 23 Å. In behavior similar to that reported for grain boundary junctions, the N-YBCO I_cR_n products scale as $J_c^{0.84}$ for current densities below 10^5 A/cm^2. For both types of devices, typical I_cR_n products at 4.2 K are limited to 1 - 2 mV at the highest current densities, possibly due to self-shielding effects.

INTRODUCTION

High temperature superconductor (HTS) Josephson devices are potentially useful for a variety of applications including high speed digital logic, Thz frequency sources and detectors, and sensitive magnetometers. One promising approach to HTS Josephson device fabrication is the use of superconductor/normal-metal/superconductor (SNS) microbridges. Such weak links generally possess nonhysteretic current-voltage (I-V) characteristics, which are well-suited for high speed logic and magnetometer applications. In addition, the utilization of a normal metal bridge can relax the severe bridge length constraints of an all-superconducting microbridge. This approach also allows control of J_c and R_n over a broad range simply by varying the normal metal bridge length.

There are a number of possible device geometries for fabrication of HTS SNS weak links including planar SNS microbridges (1,2,3,4), step-edge SNS weak links (5,6,7), sandwich-geometry SNS trilayers (8,9,10,11,12), and edge-geometry SNS weak links (13,14,15,16,17,18,19,20). This work focuses on epitaxial edge-geometry SNS weak links due to advantages associated with this approach. A schematic diagram of an edge geometry SNS weak link is shown in Figure 1. The basic device structure consists of a c-axis-oriented YBCO base electrode with an exposed edge. An epitaxial normal metal is deposited on the YBCO edge, followed by deposition of the YBCO counterelectrode. Because the top surface of the base electrode is covered by a thick insulator, electrical contact between the YBCO electrodes is confined to the edge of the lower YBCO film.

The principal advantages of the edge geometry include the facts that the critical N/S interfaces are located on the longer coherence length YBCO surfaces, current flow is along the high J_c direction parallel to the a-b planes throughout the device, and very small device areas can be produced using conventional photolithography. The edge geometry also enables very short microbridge lengths to be achieved and controlled, because the bridge length is determined by the deposited normal metal thickness. Edge junction

fabrication is somewhat simpler than for trilayer SNS devices, because the counterelectrode serves as the wiring layer and no additional insulator and wiring depositions are needed. A possible drawback of the edge geometry approach is that the ion milling process used to define the base electrode edge may cause YBCO surface damage. In addition, optimal device performance requires formation of tapered YBCO edges (discussed below). Because typical tapered edge fabrication processes produce YBCO edges with a single orientation, circuit layout can be more complex with these devices.

One of the most important factors in determining high T_c SNS device performance is the choice of which normal metal to incorporate in the device structure. In an all-epitaxial weak link, the normal metal must be lattice-matched to YBCO in order to provide a template for overgrowth of the counterelectrode. Two very important, but difficult requirements are that the normal metal be chemically compatible with YBCO at the counterelectrode growth temperature, and that the normal metal film should grow without thin spots or pinholes. A long normal metal coherence length is also desirable, and theoretical arguments suggest that the normal metal resistivity-coherence length product ($\rho_n \xi_n$) should be larger than the corresponding product for YBCO (21). These requirements severely restrict possible normal metal choices for HTS epitaxial weak links. This work examines new results with two different weak link barrier layers that meet at least some of the above constraints: ion-damaged YBCO layers and a nonsuperconducting phase of YBCO (15,16). Special attention is paid to optimization of the edge formation and edge cleaning processes, which are closely related to the ion-damaged weak links. The primary goals of this work were to develop a reliable and reproducible HTS device process, and to obtain improved HTS SNS device performance. As will be seen below, good results have been achieved using both weak link materials. However, additional improvements are still needed for some device applications, and strategies for further optimization will be discussed.

DEVICE FABRICATION

Details of the edge-geometry weak link fabrication process have been described previously (15,16,18,22), but will be briefly summarized here. Device fabrication begins with pulsed laser deposition of a c-axis-oriented YBCO thin film, typically on a LaAlO$_3$ substrate. Following growth of the base electrode, a thin (100-200 Å) MgO or cubic zirconia passivation layer is deposited over the YBCO before removal from the laser ablation chamber. Next a thick (6000-9000 Å) MgO layer is patterned using photolithography and liftoff. The patterned MgO film is utilized as an ion milling mask to produce a tapered edge in the YBCO base electrode, followed by a low energy ion cleaning step. This edge formation process is discussed in greater detail below. Just after cleaning of the YBCO edge, within the same vacuum system, the normal metal layer and YBCO counterelectrode are deposited at the appropriate growth temperatures. A lithography-ion milling step is then used to pattern via holes down to the base YBCO film and liftoff Au contact pads. Finally, another lithography-milling process defines the counterelectrode. Completed devices have counterelectrode widths ranging from 6 µm down to 1.5 µm.

EDGE CLEANING OPTIMIZATION AND ION-DAMAGED-YBCO WEAK LINKS

One of the most critical steps of edge-geometry weak link fabrication is the YBCO edge formation and cleaning process. The two key requirements for formation of the YBCO edge are: 1) that the edge must be tapered to prevent grain boundary formation in

the YBCO counterelectrode (23), and 2) that surface damage on the YBCO base electrode surface is minimized. Tapered YBCO edges are produced by Ar ion milling at an approximately 30° angle from the substrate surface (16). This angled ion milling edge cutting step is followed by a low energy ion cleaning step at normal incidence to the substrate surface. Both the edge cutting and edge cleaning steps are done in a turbo-pumped load-lock attached to the main laser ablation chamber. Between these two steps the device chip is transferred from one fixture to another inside the vented load lock under flowing N_2 gas, so that any air-exposure is minimal.

It is important to minimize ion surface damage on the YBCO base electrode edge, because such damage can result in a suppression of the energy gap in the YBCO film at the YBCO-normal metal interface, leading to a reduction of the device I_cR_n product. Edge surface damage may also result in a degradation of the quality of epitaxial overgrowth of the normal metal and counterelectrode layers. The degraded layer on the YBCO base electrode is caused by ion damage during the edge cutting and edge cleaning steps, and presumably consists of both crystalline defects and stoichiometry shifts associated with preferential ion sputtering. Shifts in oxygen stoichiometry due to oxygen loss and oxygen disorder may be especially serious problems at the YBCO-normal metal interface due to the relatively high mobility of oxygen in YBCO (24). The thickness of the YBCO damage layer is related to the energy of the impinging ions and their angle of incidence. However, it is probably not correct to simply equate the damage layer thickness with the incident ion range, because some damage may anneal out during heating in oxygen for the counterelectrode growth, and also because oxygen disordering may extend deeper than the primary ion damage depth.

In order to investigate the effect of edge ion milling and cleaning parameters, we have examined the electrical properties of devices produced with no deposited normal metal layer, where the counterelectrode is deposited directly on the ion-milled YBCO base electrode edge. These experiments were done in an effort to optimize the edge junction cleaning procedure for application to devices with deposited normal metals, and also to investigate whether high quality, controllable weak links could be produced using an ion-damaged YBCO surface layer as a "normal metal". In fact, some of the first devices fabricated without deposited normal metal layers showed excellent electrical performance, as shown in the 77 K I-V characteristics of Figure 2(a). For this weak link, the YBCO edge was produced by Ar-ion-milling at 500 eV at 30° from the substrate surface, followed by a 50 eV normal incidence Ar ion cleaning step. This device has a current density of $\approx 5 \times 10^4$ A/cm^2 at 77 K with an I_cR_n product of 153 μV and an R_nA product of 2.9×10^{-9} Ω-cm^2. The I-V characteristics are qualitatively consistent with the Resistively-Shunted-Junction (RSJ) model, although the devices on this chip do typically exhibit excess currents. The microwave response of this device is shown in Figure 2(b). Clean ac Josephson steps are seen in response to 14.4 GHz microwave irradiation with amplitudes that modulate as expected with increasing microwave power. These initial results encouraged us to investigate ion-damaged barrier weak links in more detail to see whether reproducible and controllable weak links could be produced in this manner.

As part of this study, a set of ion-damage barrier chips was fabricated using 500 eV Ar ions to etch tapered YBCO edges, followed by a normal-incidence Ar ion clean at ion energies ranging from 50 to 500 eV. The weak link electrical parameters J_c, I_cR_n, and R_nA were measured as a function of Ar ion cleaning energy. For these experiments the cleaning times were adjusted so that at each ion energy, the same total areal dose of 1.9×10^{17} ions/cm^2 was used. Figure 3 shows the dependence of the average value of J_c

on ion beam cleaning energy for four different device chips. The data shows a decrease in J_c with increasing cleaning energy up to 250 eV, as might be expected if the damage depth scales with ion range in the YBCO. However, at 500 eV, the average current density increases to a value close to that seen for the 50 eV cleaning case. This effect is not understood at this time. One point to note is that, although some variation is seen in J_c as the cleaning energy is varied, the total variation in J_c is not large. The other notable fact here is that the devices of Figure 3 exhibited RSJ-like I-V characteristics and ac Josephson steps only for cleaning energies less than or equal to 250 eV. Devices on the chip fabricated using 500 eV Ar ion cleaning showed flux-flow I-V characteristics at all temperatures and no ac Josephson steps under microwave irradiation. The lack of Josephson behavior in the 500 eV-cleaned devices probably indicates that the ion damage depth exceeds the superconducting coherence length.

The dependence of I_cR_n on the ion cleaning energy at 77 K is shown in Figure 4. The average I_cR_n products are roughly independent of cleaning energy below 250 eV, but drop off at the highest cleaning energy. The average I_cR_n values are $\approx 250~\mu V$ for the lower cleaning energies, but range up to $\approx 450~\mu V$ for some devices. These I_cR_n products are some of the highest reported for SNS weak links at 77 K. The average R_nA products for these chips were lowest for the 50 eV and 500 eV cleans, and highest at 250 eV, ranging from 3×10^{-10} to $1.7 \times 10^{-9}~\Omega\text{-cm}^2$ at 77 K. Overall, the best device and cleaning results were obtained using 50 eV Ar cleaning in combination with the 500 eV Ar edge milling step. At 4.2 K, under these conditions, for four chips (30 devices) the average J_c was $5.5 \times 10^6~A/cm^2$ with a standard deviation of $4.7 \times 10^6~A/cm^2$, the average R_nA product was $5.4 \times 10^{-10}~\Omega\text{-cm}^2$ with a standard deviation of $6.4 \times 10^{-10}~\Omega\text{-cm}^2$, and the average I_cR_n product was 1.03 mV with a standard deviation of 0.24 mV. Possible self-shielding limitations on I_cR_n are discussed in the next section. Other variations in the YBCO edge formation and cleaning process were also examined, including xenon cleaning, eliminating the ion cleaning step, and varying the edge ion mill etching energy. These process variations produced devices with parameters comparable to the weak links made using 500 eV Ar edge cutting and 50 eV Ar cleaning.

The basic conclusions of the edge formation studies are relevant to YBCO edge cleaning for application to SNS devices with deposited normal metals, as well as to fabrication of ion-damaged-YBCO SNS devices. From a cleaning perspective, the high current densities and low R_nA products found with the 50 eV Ar process indicate that this process produces very clean YBCO edges that should work well as growth templates for epitaxial normal metal devices. However, we do believe that further cleaning optimization should be possible, for example, by going to an entirely *in-situ* cleaning process. This edge formation process has also produced high quality HTS Josephson devices with ion-damaged YBCO layers serving as effective normal metal weak links. These ion-damage barrier devices have high current densities and I_cR_n products at 77 K, making them well-suited for superconducting device applications such as flux-quantum logic and SQUID magnetometers. However, this approach does have some potential drawbacks. The critical current densities of the ion-damage weak links appear to be relatively insensitive to ion cleaning energy and ion species, indicating that J_c in these devices is not controllable over a wide range. This is a problem for some cases in which control of J_c is required, such as integrated circuit applications. In some other situations, however, the insensitivity of J_c to process variations could be a significant advantage. A second potential problem is that the device current densities are approaching the electrode J_c values, which can cause difficulties with electrode transitions unless care is taken to use thick counterelectrodes. Finally, the R_nA products of the ion-damaged barrier weak

links are small, $R_nA \approx 5 \times 10^{-10}$ Ω-cm^2 at 4.2 K, so that 0.1 μm lithography will be required to produce 5 Ω devices.

N-YBCO WEAK LINKS

The edge formation and cleaning process just described provides the basis for fabrication of HTS weak links using deposited epitaxial normal metals. One possible SNS device technology uses a nonsuperconducting phase of YBa$_2$Cu$_3$O$_{7-x}$ (N-YBCO) as the normal metal. Some results on fabrication and testing of N-YBCO weak links have been presented previously (15,16). Here we examine new data on N-YBCO characterization and N-YBCO device results, including the scaling behavior of the weak link critical current densities and I_cR_n products.

The N-YBCO thin films are deposited using a standard laser ablation process and a nearly stoichiometric YBa$_2$Cu$_3$O$_{7-x}$ target, except that the films are grown at ≈ 530 C, a much lower temperature than typically used to produce high quality superconducting YBCO thin films. Because of the difficulty of characterizing N-YBCO films deposited on the very small area YBCO base electrode edge, characterization of these films has been done primarily on N-YBCO layers grown directly on LaAlO$_3$ substrates, followed by a 1-2 minute anneal at ≈ 800 C, to mimic the counterelectrode growth conditions. Lateral transport resistivity measurements on 100 Å N-YBCO thin films grown in this manner show semiconductor-like behavior, although in some cases a drop in resistance is seen near 4 K. Resistivity measurements on much thicker N-YBCO films (3000 Å) show a superconducting transition at ≈ 40 K. X-ray diffraction studies of 500 - 1000 Å thick N-YBCO show peaks consistent with orthorhombic YBa$_2$Cu$_3$O$_{7-x}$ with a c-axis lattice constant of 11.68 Å. X-ray photoelectron spectroscopy (XPS) measurements on N-YBCO films produced with the above annealing procedure show no obvious difference from standard orthorhombic YBa$_2$Cu$_3$O$_{7-x}$. Finally, preliminary high resolution cross-sectional transmission electron microscopy (HRTEM) studies give images consistent with an orthorhombic YBCO phase.

These measurements demonstrate that N-YBCO is not the semiconducting cubic phase of YBCO reported by Agostinelli et al. (25). The characterization studies also indicate that N-YBCO is probably not the the nonsuperconducting oxygen-rich (26) or oxygen-poor (27) tetragonal phases reported earlier, because these phases exhibit c-axis lattice parameters smaller or larger than the value of 11.68 Å measured from the x-ray diffraction data. It appears most likely that N-YBCO is orthorhombic YBa$_2$Cu$_3$O$_{7-x}$ with oxygen disorder suppressing the transition temperature. A number of studies have shown that YBCO is especially susceptible to oxygen movement and that oxygen disorder can significantly affect T_c (24,28,29). Presumably, crystallization of the low-temperature-deposited YBCO film occurs during the heating ramp to the counterelectrode growth temperature, but sufficient oxygen disorder, and possibly other point defects remain to suppress superconductivity in these films. This supposition is consistent with device results indicating that SNS coupling through N-YBCO is sensitive to the high temperature counterelectrode growth parameters. In particular, we find that weak link current densities increase for hotter counterelectrode growth temperatures. These results suggest that N-YBCO is metastable, and that increased high temperature annealing results in reduced crystalline disorder and stronger weak link coupling. At room temperature, however, the N-YBCO devices are very stable, with almost no change in the current-voltage characteristics after more than a year of storage in an Ar-filled desiccator.

As reported previously (15,16), SNS weak links fabricated with N-YBCO normal metal layers typically exhibit RSJ-like current-voltage characteristics with some excess current. These devices show clean ac Josephson steps at 14.4 GHz, which modulate as expected with increasing microwave power. Studies of the magnetic field dependence of the critical currents in N-YBCO SNS weak links show Fraunhofer-like patterns with 30 - 90% modulation (16). This magnetic field behavior demonstrates good large scale barrier uniformity, but the incomplete modulation is consistent with fine scale nonuniformities in the N-YBCO or the N-S interfaces. Figure 5 is a plot of the average SNS weak link current density for the devices on 25 chips at 4.2 K as a function of the N-YBCO barrier thickness. The straight line is a fit to the data for N-YBCO thicknesses less than or equal to 100 Å, showing that J_c scales exponentially with barrier thickness in this range, with an effective normal metal coherence length of 23 Å. Devices with N-YBCO layers thicker than $\approx$ 100 Å suffer from degraded counterelectrode quality with lower transition temperatures and higher resistivities. For these devices, a more rapid decrease in J_c with increasing barrier thickness is seen due to the degradation of the counterelectrode properties. This deterioration in the quality of the YBCO counterelectrode suggests that there is an epitaxial growth problem on N-YBCO barriers over 100 Å, presumably because these layers are not providing a good epitaxial growth template for counterelectrode overgrowth. This problem may be eliminated by more careful optimization of the N-YBCO growth and annealing conditions.

Another potential problem with these devices is the variation in device properties. Critical current density standard deviations across a single quarter inch chip were as small as 18%, and typically ranged from 20 - 100%. However, as much as an order of magnitude variation in critical currents was seen from chip to chip for a given barrier thickness, and the J_c standard deviations for all devices from all chips at each N-YBCO thickness ranged from $\approx$ 70% to 200%. Some of this variability can be attributed to process variations which were investigated during various device fabrication runs. In addition, the short coherence length and metastable nature of N-YBCO make these weak links especially susceptible to planned or unplanned process changes. Tighter process control is expected to help improve reproducibility.

We have also examined the scaling behavior of I_cR_n as a function of J_c for both the N-YBCO and ion-damage barrier devices, as shown in Figure 6. A fit to the data for $J_c <$ 10^5 A/cm^2 indicates that I_cR_n scales as $J_c^{0.84}$ over a wide range of current densities. This scaling behavior is similar to that reported for grain boundary weak links and is evidence that transport in these devices occurs through superconducting filaments shunted by normal regions (24). Such nonuniform conduction could result from oxygen disorder in the N-YBCO layers or in the ion-damaged surface layer on the YBCO base electrode. This superconducting filament model is consistent with the magnetic field modulation studies of the critical currents, which pointed to fine scale nonuniformities in these devices. The second important point to note about the data of Figure 6 is that the I_cR_n products for most devices saturate at $\approx$ 1-2 mV above 10^5 A/cm^2. This effect is probably due to self-shielding effects in these very high J_c devices: we calculate a Josephson penetration depth of $\approx$ 1 μm at 10^5 A/cm^2 and our minimum device width is 1.5 μm. In fact, a replotting of the data (not shown) indicates that the smaller devices do have higher I_cR_n products at the highest current densities. We plan to fabricate smaller devices using electron beam lithography in an attempt to reproducibly obtain higher I_cR_n products. In addition, we are also examining other epitaxial normal metal layers such as $PrBa_2Cu_3O_{7-x}$ (18) in order to achieve improved weak link reproducibility and higher I_cR_n products at lower current densities.

SUMMARY

We have fabricated and tested HTS edge-geometry weak links utilizing ion-damaged YBCO and a nonsuperconducting phase of YBCO (N-YBCO) as weak link barrier materials. Special attention was focused on optimization of the YBCO base electrode edge formation and cleaning process. It was found that high quality YBCO edges could be prepared using a 500 eV Ar edge milling step in combination with 50 eV Ar cleaning. When used to fabricate weak links with no deposited barrier layer, in which the remnant ion damage serves as the weak link barrier, this cleaning process produced devices with average values of $J_c = 5.5 \times 10^6$ A/cm^2 and average R_nA products of 5.4×10^{-10} Ω-cm^2. The ion-damaged weak links exhibited good quality RSJ I-V characteristics, but could only be fabricated over a relatively limited current density range approaching the YBCO electrode J_c values. We have also produced SNS weak links using N-YBCO layers as the normal metal barrier. Characterization of the N-YBCO films suggests that this material is the orthorhombic phase of $YBa_2Cu_3O_{7-x}$ with oxygen disorder and possibly other point defects suppressing T_c. The N-YBCO weak links show RSJ I-V characteristics with strong microwave and magnetic field response. The critical currents of the N-YBCO devices scale exponentially with barrier thickness for barriers less than 100 Å with a nominal coherence length of 23 Å. The I_cR_n products of these devices are usually limited to 1 - 2 mV, and scale as $J_c^{0.84}$ in behavior similar to that reported for grain boundary junctions, suggesting that transport may be dominated by superconducting filaments shunted by normal regions. The I_cR_n scaling behavior also indicates that higher I_cR_n products may be obtained by fabricating smaller devices at the highest current densities.

AKNOWLEDGEMENTS

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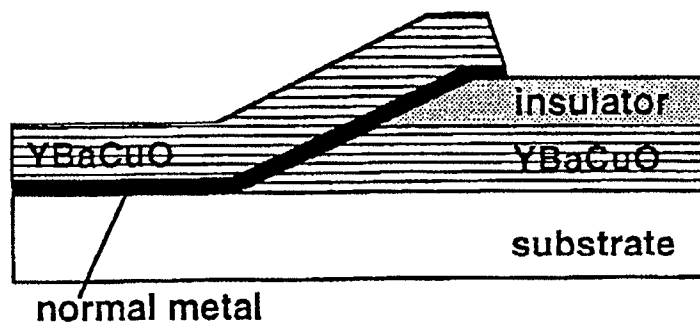
Figure 1. Cross-sectional schematic diagram of edge-geometry SNS weak link.

(a)

(b)
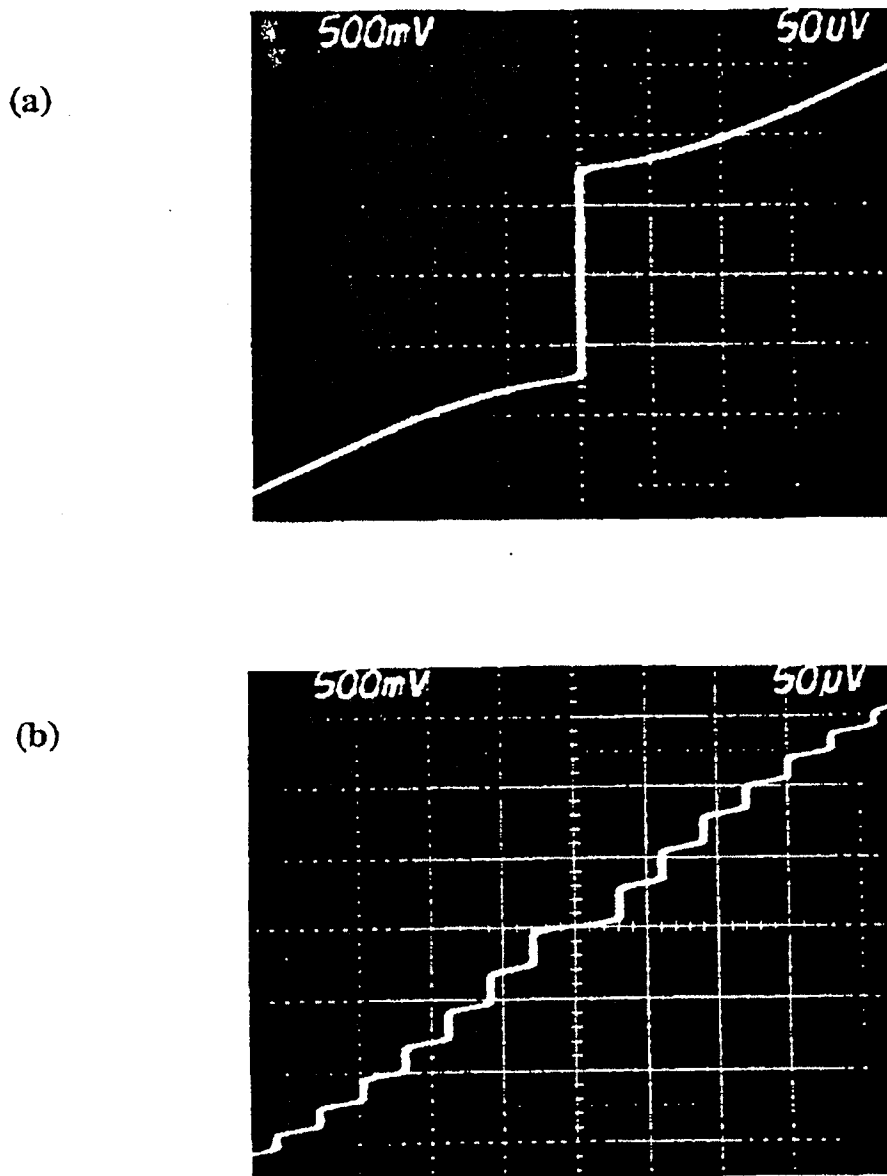
Figure 2.   (a) Current-voltage characteristics at 77 K of ion-damaged YBCO weak link produced by Ar-ion milling at 500 eV, and cleaned *in-situ* with 50 eV Ar ions. The device size is 3 µm x 0.46 µm, $J_c = 5 \times 10^4$ A/cm^2, $I_cR_n = 153$ µV, and $R_nA = 2.9 \times 10^{-9}$ Ω-cm^2. (b) Microwave response of ion-damage weak link at 14.4 GHz. For both I-Vs the vertical scale is 0.5 mA/div. and the horizontal scale is 50 µV/div.
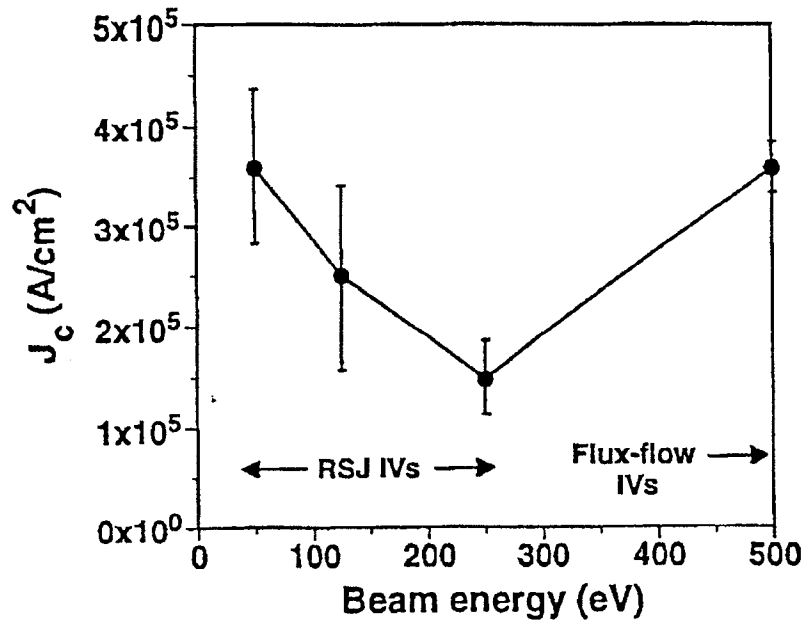
Figure 3. Plot of the average J_c versus Ar cleaning energy at 77 K for weak links on four chips produced with a 500 eV Ar edge cutting process and no deposited barrier layer. The error bars give the standard deviation in J_c for each chip.
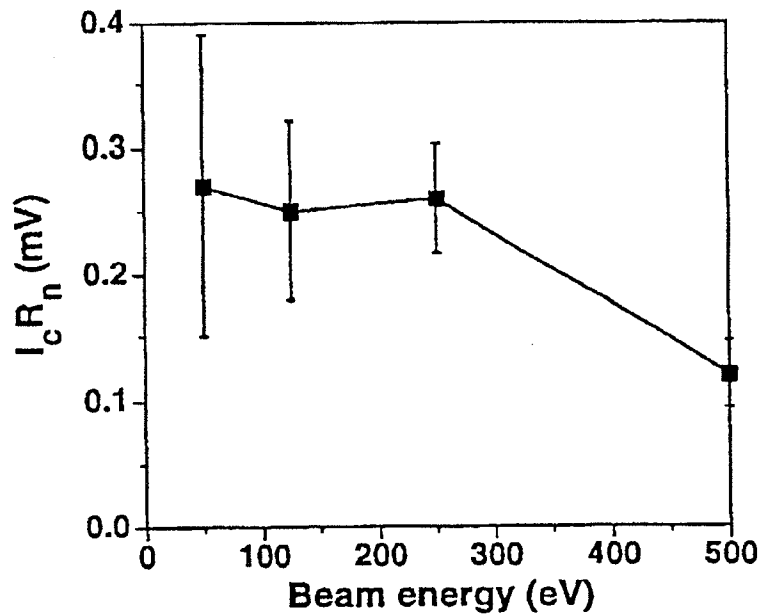
Figure 4. Plot of the average I_cR_n product versus Ar cleaning energy at 77 K for weak links on four chips produced with a 500 eV Ar edge cutting process and no deposited barrier layer. The error bars give the standard deviation in I_cR_n for each chip.
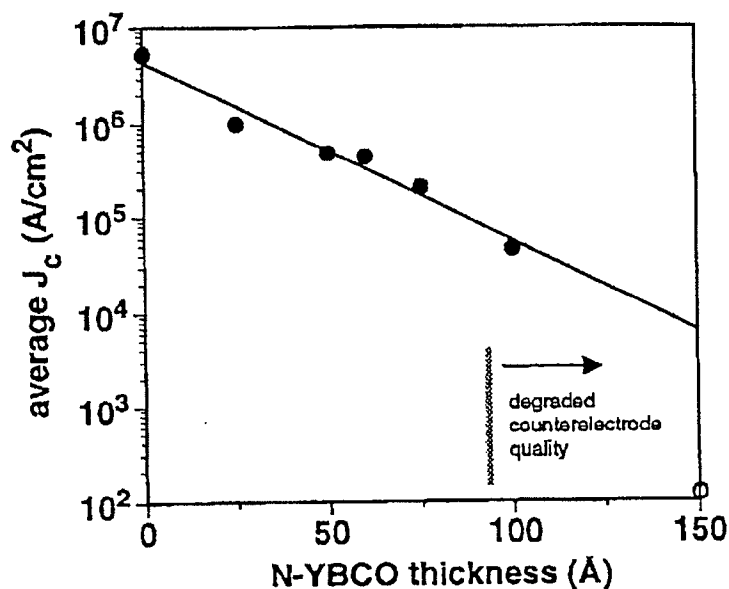
Figure 5. Plot of the average critical current density vs. N-YBCO thickness for 25 chips at 4.2 K. The line is a fit to $J_c = \exp(-L/\xi_n)$ for barrier thicknesses, L, less than or equal to 100 Å (solid points), and $\xi_n \approx 23$ Å is the effective normal metal coherence length.
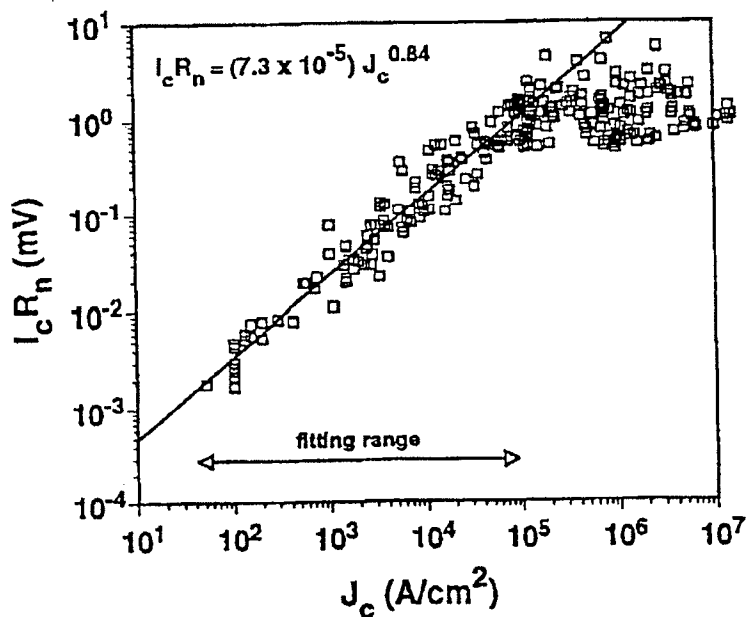
Figure 6. A plot of $I_c R_n$ vs J_c for N-YBCO and ion-damage barrier devices on 33 chips at 4.2 K. The line is a fit to the data for $J_c < 10^5$ A/cm^2, indicating that $I_c R_n$ scales as $J_c^{0.84}$ in this range.

ECS '93 And Spring MRS '93

Edge Cleaning Optimization and Ion-Damaged Barrier Weak Links

- **Basic edge cutting and cleaning process:**

1) Ion mill at 60° angle to produce tapered YBCO edge.

2) "Quasi-in-situ" transfer inside N_2-purged load-lock.

3) Normal incidence, low E ion clean.

4) Heat in O_2 for YBCO counterelec. growth.

Clean edge   Cut Edge
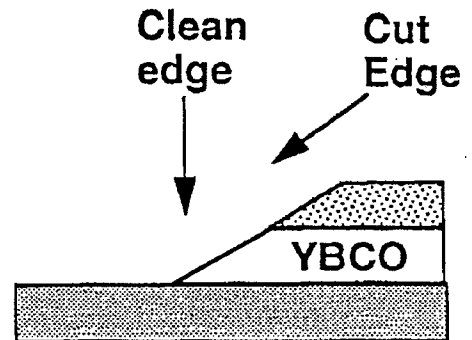
YBCO

- Looking in the limit of **zero barrier thickness,** where the YBCO counterelectrode is deposited directly on the ion-milled base electrode edge.

- We have examined the dependence of the edge junction electrical properties on the edge cutting and cleaning parameters in this limit of "no barrier" in order to:

1) Optimize the cleaning procedure to obtain the cleanest possible YBCO-normal metal interface in weak links using deposited normal metals.

2) Investigate whether high quality, controllable weak links could be produced using an ion-damaged YBCO surface layer as a "normal metal"

8   *Brian Hunt*

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Edge-Geometry, All-YBCO Weak Links with Ion-Damaged Barrier Layers

- YBCO edge produced by Ar-ion milling at 500 eV, and cleaned in-situ at 50 eV.

- T = 77 K;   Device size is 3 μm x 0.46 μm

$J_c = 5.3 \times 10^4$ A/cm^2

$I_c R_n = 153$ μV (1.3 mV - 4.2K)

$R_n A = 2.9 \times 10^{-9}$ Ω-cm^2

(Ic=0.73mA, Rn=0.21Ω)
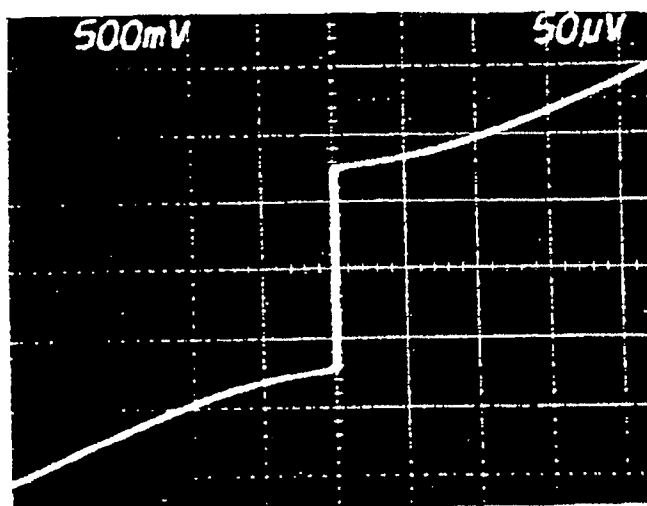
0.5 mA/div.   50 μV/div.

ac Josephson effect at 14.4 GHz

Step amplitudes vs RF field qualitatively consistent with theory.

9
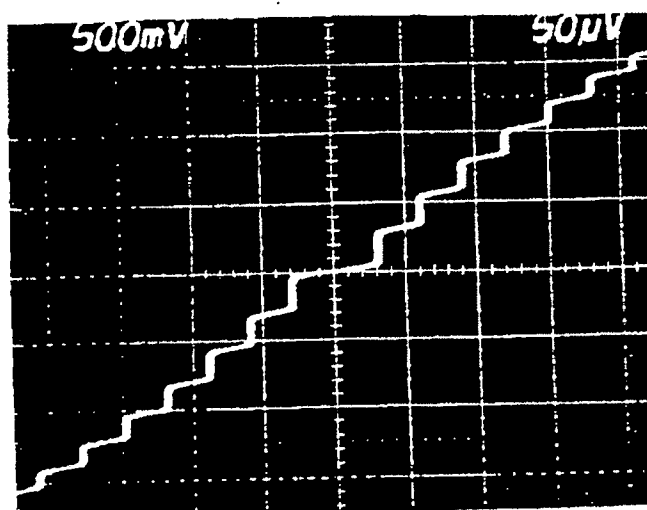
Dependence on Edge Cleaning Parameters

- **Examine J_c, I_cR_n, and R_nA as a function of Ar ion cleaning energy following 500 eV Ar edge mill:**

J_c vs Ar Cleaning Energy at 77 K
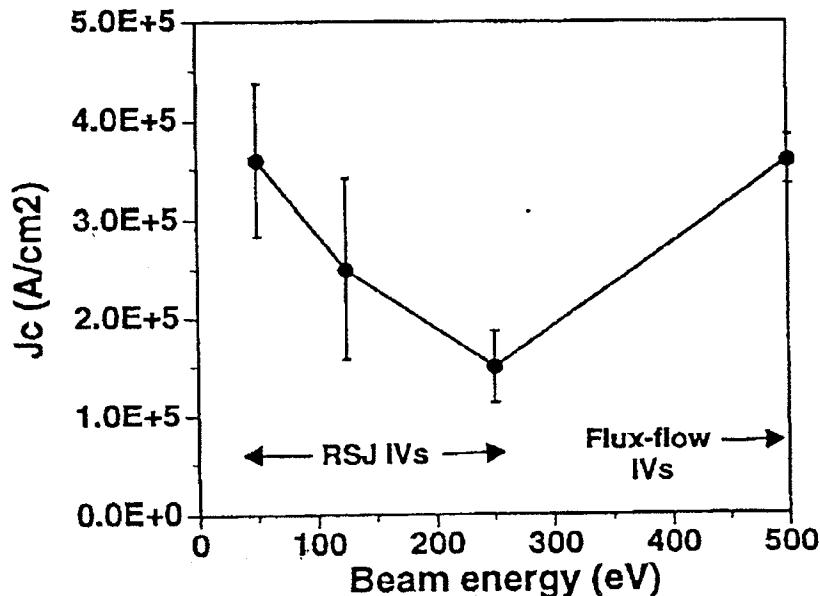
I_cR_n vs Ar Cleaning Energy at 77 K
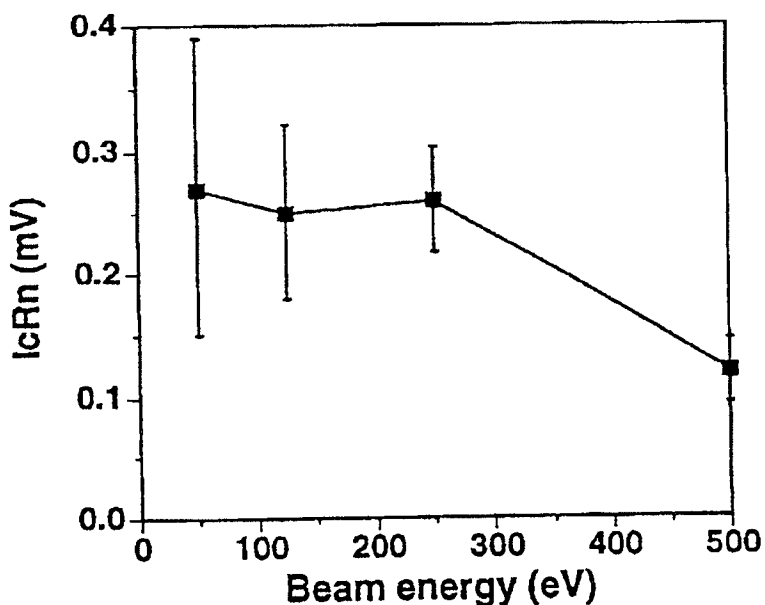
For 500 eV Ar edge cutting, 50 eV Ar cleaning gives best overall results

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YBCO Edge Cleaning Results

- ## For 500 V Ar milling and 50 V cleaning at 4.2K:

  - Ave. J_c = 5.5 x 10^6 A/cm^2 ± 4.7 x 10^6 A/cm^2

  - Ave. R_nA = 5.4 x 10^{-10} Ω-cm^2 ± 6.4 x 10^{-10} Ω-cm^2

  - Ave. I_cR_n = 1.03 mV ± .24 mV*

  *Note that I_cR_n may be limited by self-shielding effects in these very high J_c devices.

- ## We have also tried:

  1) **Xenon cleaning** --> Xe has ≈ 1/3 the range of Ar resulting in shallower surface damage - No significant difference seen.

  2) **Eliminating the ion cleaning step** - No significant difference seen.

  3) **Varying the edge cutting energy** - Lowering edge milling energy to 250 eV produced no real improvement.

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Edge Cleaning Studies - Conclusions

● **<u>Ion-Damaged Barrier Weak Link Fabrication</u>:**

   ◆ **Excellent quality IVs at 77K ... may be useful for some applications.**

   ◆ **However, this approach does have drawbacks:**

      » **J_c is not controllable over wide range** (advantage?)

      » **Device J_c is approaching electrode J_c --> can have problems with electrode transitions.**

      » **R_nA products are small $\approx 5 \times 10^{-10}$ Ω-cm^2 --> need 0.1 μm lithography for 5 Ω devices.**

● **<u>Edge Cleaning Optimization</u>:**

   ◆ **Process produces very clean edges with high J_c (5.5 x 10^6 A/cm^2) and low R_nA (5 x 10^{-10} Ω-cm^2) at 4.2K.**

   ◆ **Measured I_cR_n products at 4.2K are $\approx$ 1mV.** (limited by self-shielding effects?)

   ◆ **Futher optimization should be possible.**

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USSN 10/751,091

EVIDENCE APPENDIX

ATTACHMENT B.4

Effect of chemical and ion-beam etching on the atomic structure of interfaces in $YBa_2Cu_3O_7$/$PrBa_2Cu_3O_7$ Josephson junctions

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The atomic structure of the interfaces of Josephson junctions formed by epitaxial $YBa_2Cu_3O_7$/$PrBa_2Cu_3O_7$/$YBa_2Cu_3O_7$ triple-layer films was investigated by high-resolution transmission electron microscopy. The samples were fabricated by sputter deposition on surfaces which were etched *ex situ* either chemically, using a nonaqueous Br-ethanol solution, or by an Ar ion beam. In the interfaces produced after ion etching a thin intermediate layer with a thickness of a few nanometers was observed. The main part of this layer consists of cubic $PrBa_2Cu_3O_7$ or $YBa_2Cu_3O_7$ which is cation disordered. The interfaces formed during deposition on Br-ethanol-etched surfaces did not contain such an intermediate layer but exhibited high structural perfection similar to that of interfaces produced *in situ*. These observations permit a qualitative explanation of the difference in the electrical properties of junctions produced by these two techniques. © *1995 American Institute of Physics.*

Multilayer Josephson junctions are now routinely fabricated on the basis of $YBa_2Cu_3O_7$ in the classical way by sandwiching a thin layer of nonsuperconducting material between two superconducting layers. In this instance, constraints arise for the barrier materials employed and for the fabrication processes used due to the need to maintain perfect epitaxy throughout the multilayer system. In order to obtain optimum electrical characteristics of the junctions, a possible structural and chemical degradation of the superconducting layers must be limited to a very narrow zone at the interfaces. The particular design of the multilayer edge- or ramp-type junction favors tunneling parallel to the ab-plane where the coherence length is maximum. In most cases $PrBa_2Cu_3O_7$ is employed as nonsuperconducting barrier material.[1,2] Its structure is isomorphic to that of the superconductor and the lattice mismatch of the two materials is small.

In the fabrication of electronic devices and circuits, *ex situ* processing steps are involved. In particular patterning, in general, has to be carried out outside the laser or sputter system used for deposition of the individual layers. The structural perfection, residual damage level, and chemical constitution of the surfaces largely depend on the processing technology. The current patterning technology for edge-type Josephson junctions is based on either ion-milling[3,4] or chemical etching.[5] However, the electrical properties reported for $YBa_2Cu_3O_7$/$PrBa_2Cu_3O_7$/$YBa_2Cu_3O_7$ Josephson junctions and for electrical $YBa_2Cu_3O_7$/$YBa_2Cu_3O_7$ connects (without $PrBa_2Cu_3O_7$ barrier layer) fabricated by using these two techniques differ considerably. Since the performance of the chemically etched junctions is in general superior to those fabricated involving ion milling the present electron microscopic investigation was carried out in order to search for possible characteristic structural differences of the interfaces produced by these two techniques.

Test samples consisting of $YBa_2Cu_3O_7$/$PrBa_2Cu_3O_7$/$YBa_2Cu_3O_7$ triple layers were prepared on (001) $SrTiO_3$ substrates by the high-oxygen pressure dc-sputtering technique.[6] The interfaces between the two compounds were produced on the basis of two *ex situ* processing steps. As sketched in Fig. 1 (sample type 1), the first, i.e., the lower interface was formed by deposition of the $PrBa_2Cu_3O_7$ layer on a Br-ethanol-etched surface of the first $YBa_2Cu_3O_7$ layer.[5] The second, i.e., the upper interface was created by the deposition of $YBa_2Cu_3O_7$ on the $PrBa_2Cu_3O_7$ layer etched by an Ar ion beam. Its energy was 600 eV and the ion-current density 50 $\mu A/cm^2$, resulting in an etching rate of about 2 nm/min. After each etching treatment the samples were annealed in oxygen atmosphere (pressure 3 mbar) at 800 °C for 30 min prior to the deposition of the subsequent layer. The test samples of type 2 were produced by inverting the sequence of the two types of etching steps, i.e., the fabrication of the lower interface involved the Ar ion etching step and the upper interface the Br-ethanol step. For comparison, a third type of samples was produced by an *in situ* technique in a dual-target sputtering system without Ar ion or chemical etching under otherwise identical conditions.

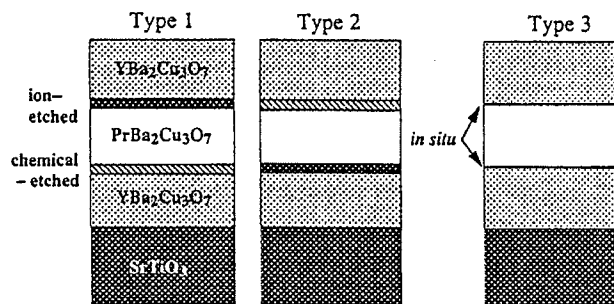Figure 2 shows a low-magnification lattice fringe picture

FIG. 1. Schema of the cross-sectional sample geometry. Type 1: lower $YBa_2Cu_3O_7$/$PrBa_2Cu_3O_7$ interface formed on a Br-methanol-etched surface; upper $PrBa_2Cu_3O_7$/$YBa_2Cu_3O_7$ interface formed on an ion-beam-etched surface. Type 2: ion-beam irradiation for the lower and chemical etching for the upper interface. Type 3: *in situ* preparation by dual-target sputtering system.
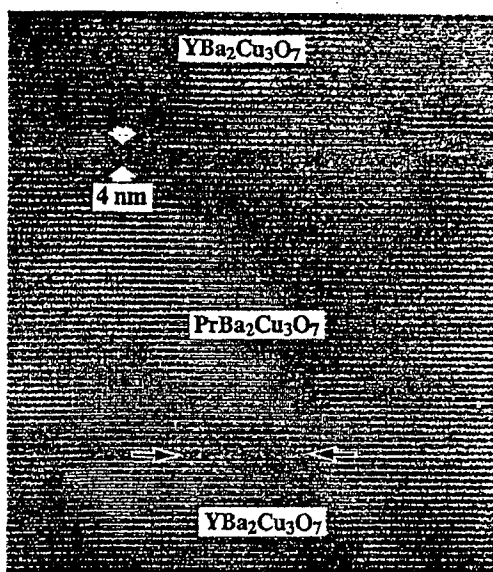
FIG. 2. A low-magnification overview of the YBa$_2$Cu$_3$O$_7$/PrBa$_2$Cu$_3$O$_7$/YBa$_2$Cu$_3$O$_7$ triple layer of sample type 1. The upper and lower interface is based on the ion-etched surface and the Br-ethanol-etched surface, respectively.

of the triple-layer system of sample type 1 with its (vertical) c axis perpendicular to the (001) surface of the SrTiO$_3$ substrate (not shown). The lower interface (horizontal arrows), between the first YBa$_2$Cu$_3$O$_7$ layer and the central PrBa$_2$Cu$_3$O$_7$ layer, is that obtained after chemical etching. The upper interface, between the PrBa$_2$Cu$_3$O$_7$ layer and the second YBa$_2$Cu$_3$O$_7$ layer, is the one obtained after ion-beam etching. A clear difference in the image contrast of the two interfaces can be recognized. The lower interface looks sharper than the upper one. The latter includes a thin interface layer a few nanometers thick as indicated by a pair of white vertical arrows. Nevertheless, good epitaxy is maintained across all three layers. In some regions, a-axis oriented grains of YBa$_2$Cu$_3$O$_7$ were found to grow from the thin interface layer to a thickness of about 10 nm after which they were overgrown by the c-axis oriented film. The interface layer was also observed in the ion-etch-related lower interface of the second type of test sample.

At the lower interface in Fig. 2, the YBa$_2$Cu$_3$O$_7$ and PrBa$_2$Cu$_3$O$_7$ layers connect very well. A detailed investigation of many different samples showed that the structure is essentially perfect over more than 80% of the interface area. The observed fault structures are as follows: Occasionally contrast irregularities occur horizontally over areas extending over about 30 nm (black arrows). The irregularities are, however, vertically restricted to a distance of a single c-axis lattice parameter. Stacking faults with a double CuO chain plane are also occasionally observed. This type of defect is well known and frequently observed in homogeneous YBa$_2$Cu$_3$O$_7$ films. In addition, such stacking faults are also found at or near the interfaces in YBa$_2$Cu$_3$O$_7$/PrBa$_2$Cu$_3$O$_7$ multilayer or superlattice films prepared in situ.[7] In general, no difference between the best in situ interfaces and the Br-ethanol-etched interfaces was found.
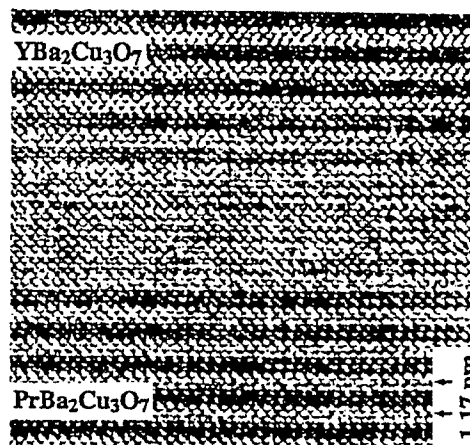

FIG. 3. Lattice image of the interface layer related to the ion-etched surface of the PrBa$_2$Cu$_3$O$_7$ layer.

The upper ion-etch-related interface is shown in greater detail in Fig. 3. The atomic structure of the extra interface layer is well-defined. The structure clearly differs from that in the adjacent PrBa$_2$Cu$_3$O$_7$ and YBa$_2$Cu$_3$O$_7$ areas, giving rise to a simple square contrast pattern. Energy-dispersive x-ray spectroscopy in the interface layer indicated that the layer has the same 123 stoichiometry as the perfect Pr-based compound. For the lower interface of sample type 2, where the YBa$_2$Cu$_3$O$_7$ layer was ion-beam etched prior to the deposition of the Pr compound, we find the same structure as in Fig. 3. A detailed analysis of different areas of the ion-etch-related interfaces in several samples showed that the square contrast is dominant. However, in some areas a few traces of the c-axis fringe pattern typical for YBa$_2$Cu$_3$O$_7$ or PrBa$_2$Cu$_3$O$_7$ can still be recognized. For example, in Fig. 4 the c-lattice periodicity of the PrBa$_2$Cu$_3$O$_7$ layer (sample type 1) is continued through the region in the interface layer between the two arrows.

The unit-cell dimension in the square pattern is the same as that of the Ba centered perovskite subunit cells of the Y or Pr compound. Therefore, the image is also compatible with a unit cell of those viewed down the c-axis direction, i.e., the image of an a-axis oriented grain in a c-axis oriented film matrix. This possibility can, however, be ruled out on the
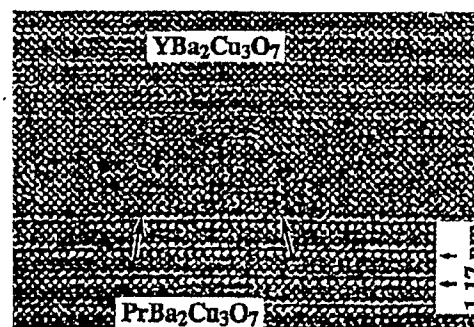

FIG. 4. High magnification of an area (between the two arrows) of the interface layer where the image contrast of the "normal" c-lattice period is visible but weaker than that in the perfect YBa$_2$Cu$_3$O$_7$ and PrBa$_2$Cu$_3$O$_7$ layers.

basis of a simple statistical argument. If the interface layer consisted of a-axis oriented grains we would expect two basically different lattice orientations which, since the samples for electron microscopy were prepared with no special preference for any of these two possibilities, should occur with equal probability. In the first, the "top view" of the $YBa_2Cu_3O_7$ or $PrBa_2Cu_3O_7$ unit cell (this is already discussed), the c axis is along the viewing direction. In the second, the "side view," the c-axis direction is rotated by 90° about the film normal.

Therefore, we conclude that the extra layer in the ion-beam-prepared interface consists of cubic $PrBa_2Cu_3O_7$ or $YBa_2Cu_3O_7$ which is disordered with respect to the cations. Indeed it could be shown that irradiation of $YBa_2Cu_3O_7$ by ions can damage the crystal structure and suppress superconductivity, depending on the energy and fluence of the ions used.[8–10] The first effect, the structural damage, is also expected for the isomorphous $PrBa_2Cu_3O_7$ compound. The ion energy used in the present study was low. Therefore, only a very thin layer below the surface is expected to contain damage at the end of irradiation.

Our study shows that the annealing treatment at 800 °C in oxygen atmosphere does not restore the perfect lattice structure of the ion-beam-damaged film. To our knowledge, the recovery of structural damage in thin films ion irradiated at low ion energies has not been studied in any detail in the literature, either for the Pr compound or for the Y compound. The only recovery data available concern $YBa_2Cu_3O_7$ irradiated by high-energy ions.[9,10] At annealing temperatures between 750 and 800 °C an a-axis oriented film and, at higher temperatures, a c-axis film was found to form on (001) oriented substrates. We note that a cubic structure with a unit cell dimension of about 1/3 $YBa_2Cu_3O_7$ is known from studies of low-temperature deposition of $YBa_2Cu_3O_7$, i.e., at 580–620 °C.[11]

The results obtained in the present work may be used for a qualitative explanation of the different electrical properties of the $YBa_2Cu_3O_7/PrBa_2Cu_3O_7$ junctions prepared by chemical and ion-beam etching.[3–5] The interfaces produced involving Br-ethanol etching are essentially of the same structural quality as those produced by the *in situ* technique which leads to abrupt and coherent interfaces. On the other hand, the deposition of $PrBa_2Cu_3O_7$ on an ion-beam etched and annealed $YBa_2Cu_3O_7$ surface produces an additional layer of cubic and cation-disordered $YBa_2Cu_3O_7$. Cubic $YBa_2Cu_3O_7$ is semiconducting or effectively isolating with electronic properties quite different from those of $PrBa_2Cu_3O_7$. As a result, the ion-beam-etched junctions show an electrical behavior different from that of the chemically etched junctions.

Finally, we note that Josephson junctions of the edge-junction design have recently been successfully produced by using $YBa_2Cu_3O_7$ deposited at low temperature as the normal layer.[12] This corroborates our view that the occurrence of the cubic Y compound in the ion-beam-etched interfaces leads to junctions which are structurally and electrically more complex than the chemically etched junctions with appropriate consequences for the junction performance.

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